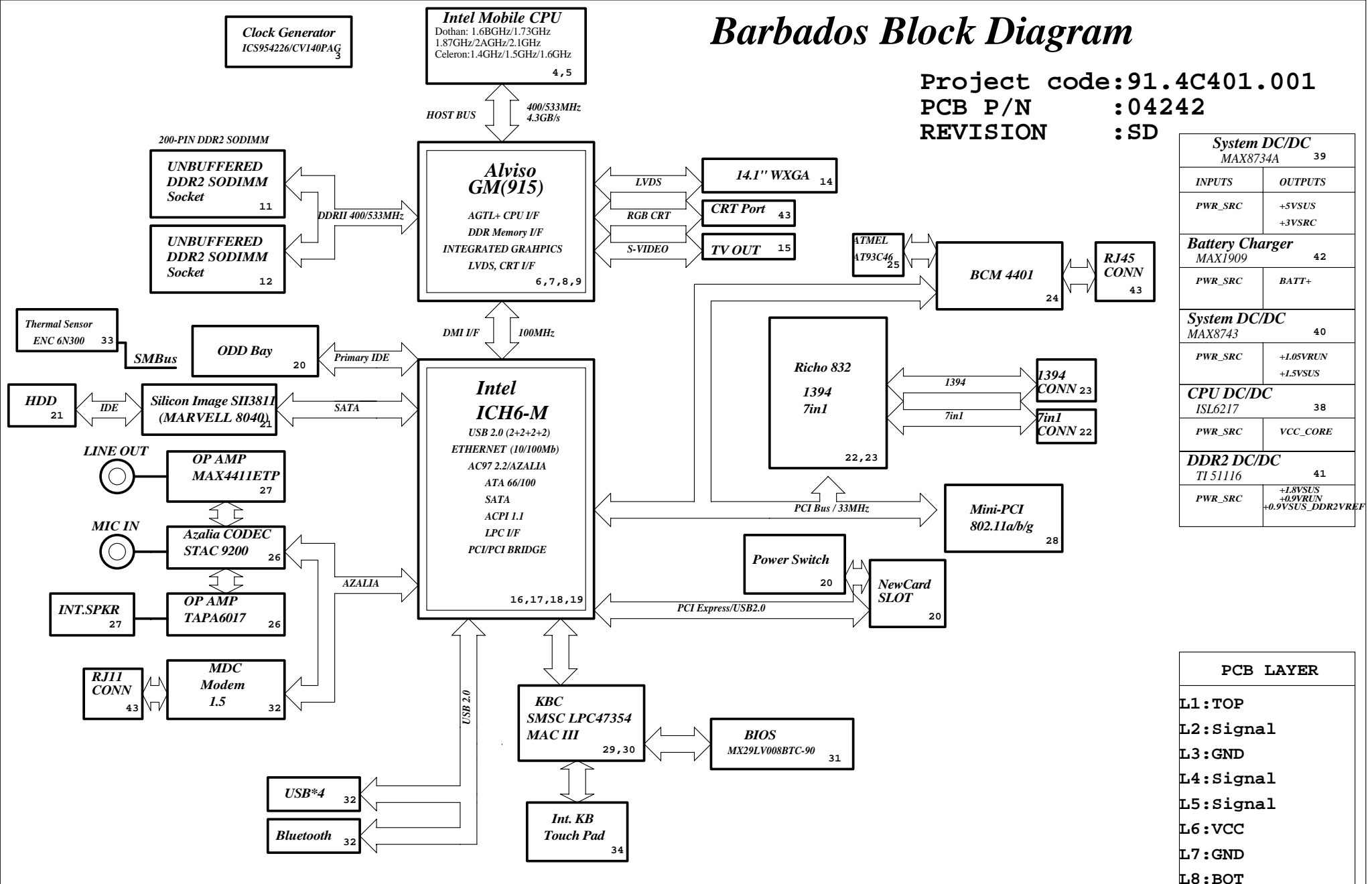


Barbados Block Diagram

Project code: 91.4C401.001
PCB P/N : 04242
REVISION : SD



System DC/DC MAX8734A 39	
INPUTS	OUTPUTS
PWR_SRC	+5VSUS +3VSRC
Battery Charger MAXI909 42	
PWR_SRC	BATT+
System DC/DC MAX8743 40	
PWR_SRC	+1.05VRUN +1.5VSUS
CPU DC/DC ISL6217 38	
PWR_SRC	VCC_CORE
DDR2 DC/DC TI 51116 41	
PWR_SRC	+1.8VSUS +0.9VRUN +0.9VSUS_DDR2VREF

PCB LAYER
L1:TOP
L2:Signal
L3:GND
L4:Signal
L5:Signal
L6:VCC
L7:GND
L8:BOT

Wistron/Dell confidential

Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK in signal.

ICH6-M Strapping Signals and Configuration

Pin Name	Strap Description	Note
ACZ_SDOUT	0=Normal(default) 1=XOR Test mode	
ACZ_SYNC	0=Normal(default)	1=Reserved
DPRSPLVR	0=Normal	1=Reserved
EE_CS	0=Normal	1=Reserved
EE_DOUT	0=Normal	1=Reserved
GNT[5]#/GPO[17]#	0=PCI cycles to FWH 1=PCI cycles to LPC (default)	Selects memory range to FWD to out of PCI
GNT(6)#/GPO(16)#	0="Top block swap" mode 1=Normal(default)	"Top block swap" inverts A16 on cycles to FWH
GPIO[25]	0=Internal 2.5V DISEN(default) 1=ENABLE Internal Vcc2_5VRM	
INTVRMEN	0=Internal VccSus1.5V DISEN (default) 1=ENABLE Internal VccSus1.5VVRM	
LINKALERT#	1=Normal(requires external PU)	0=Reserved
REQ[4:1]	XOR Test Chain Selection	Requires external resistors
SATALED#	0=Normal(default)	1=Reserved
SPKR	0=Normal(default) 1=NO Reboot	
TP[3]	0=Enter XOR Test mode 1=Normal(default)	

NOTE: All strap signals are sampled on the rising edge of the ICH6-M's PWROK signal.

BATT+	BATT+	42,43	+0.9VSUS_DDR2VREF	+0.9VSUS_DDR2VREF	7,11,12,41,44
DC_IN+	DC_IN+	42,43,44	+5VSUS	+5VSUS	18,26,27,32,33,36,39,40,41,43,44
PWR_SRC	PWR_SRC	14,29,38,39,40,41,42,43,44	+3VSUS	+3VSUS	14,17,18,19,20,24,25,27,28,32,33,35,36,39,40,41,43,44
VCCRTC	VCCRTC	16,18,29,33	+1.5VSUS	+1.5VSUS	18,36,40,44

For Dothan B stepping

	CPU		NB		CLOCK			
	BSEL1	BSEL0	CFG2	CFG1	CFG0	FS_C	FS_B	FS_A
100MHZ	0	1	1	0	1	1	0	1
133MHZ	0	0	0	0	1	0	0	1

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
LAN Broadcom BCM4401/BCM5507	AD16	PIRQC#	REQ4# / GNT4#
MINIPCI SLOT	AD19	PIROB# PIRQD#	REQ3# / GNT3#
R5C832	AD17	PIRQA# PIRQC#	REQ1# / GNT1#

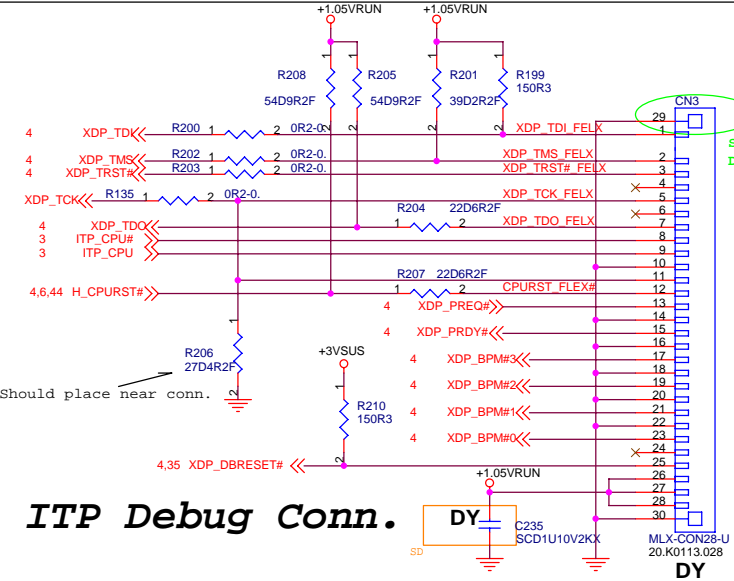
ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDRQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------



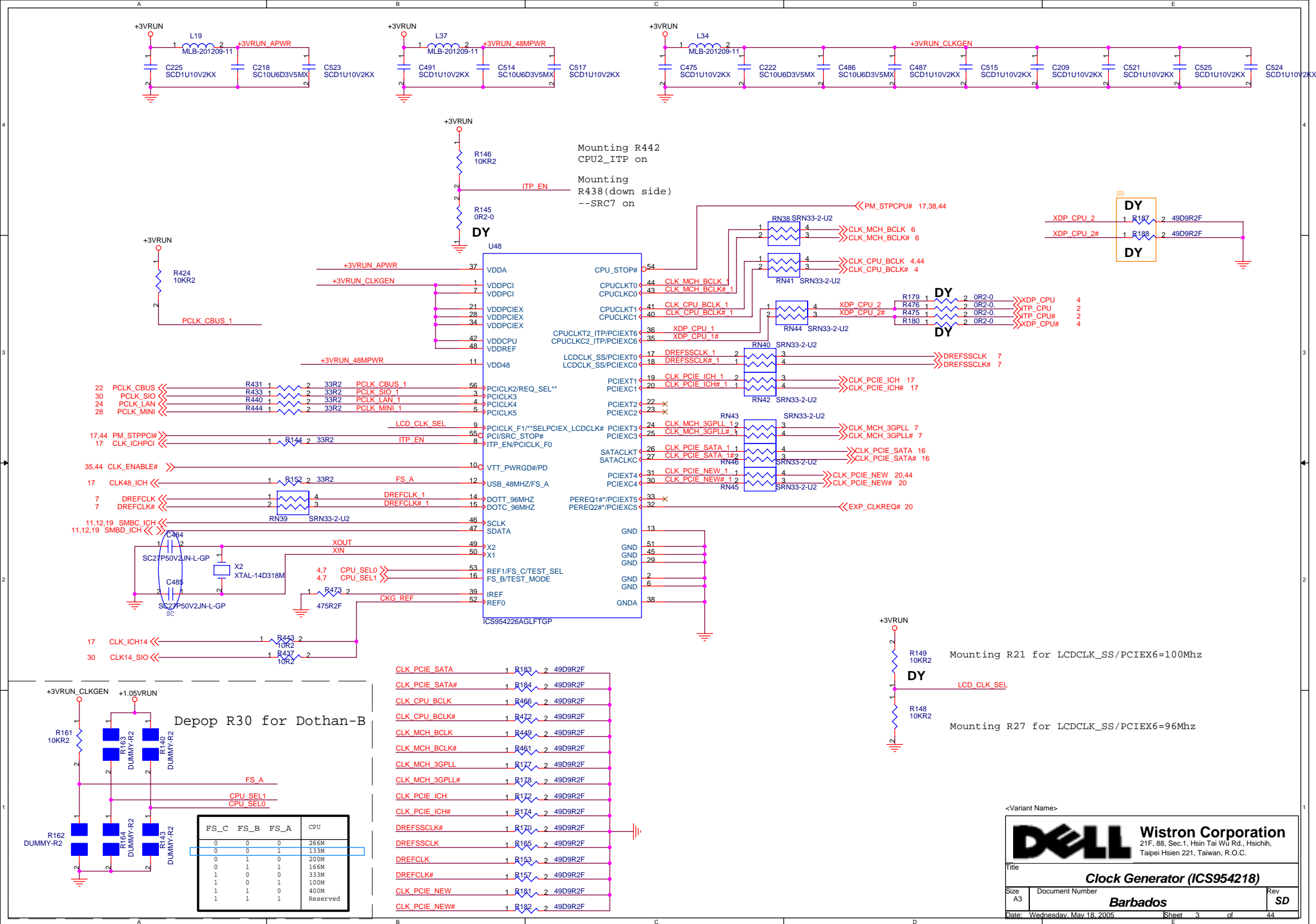
ITP Debug Conn.

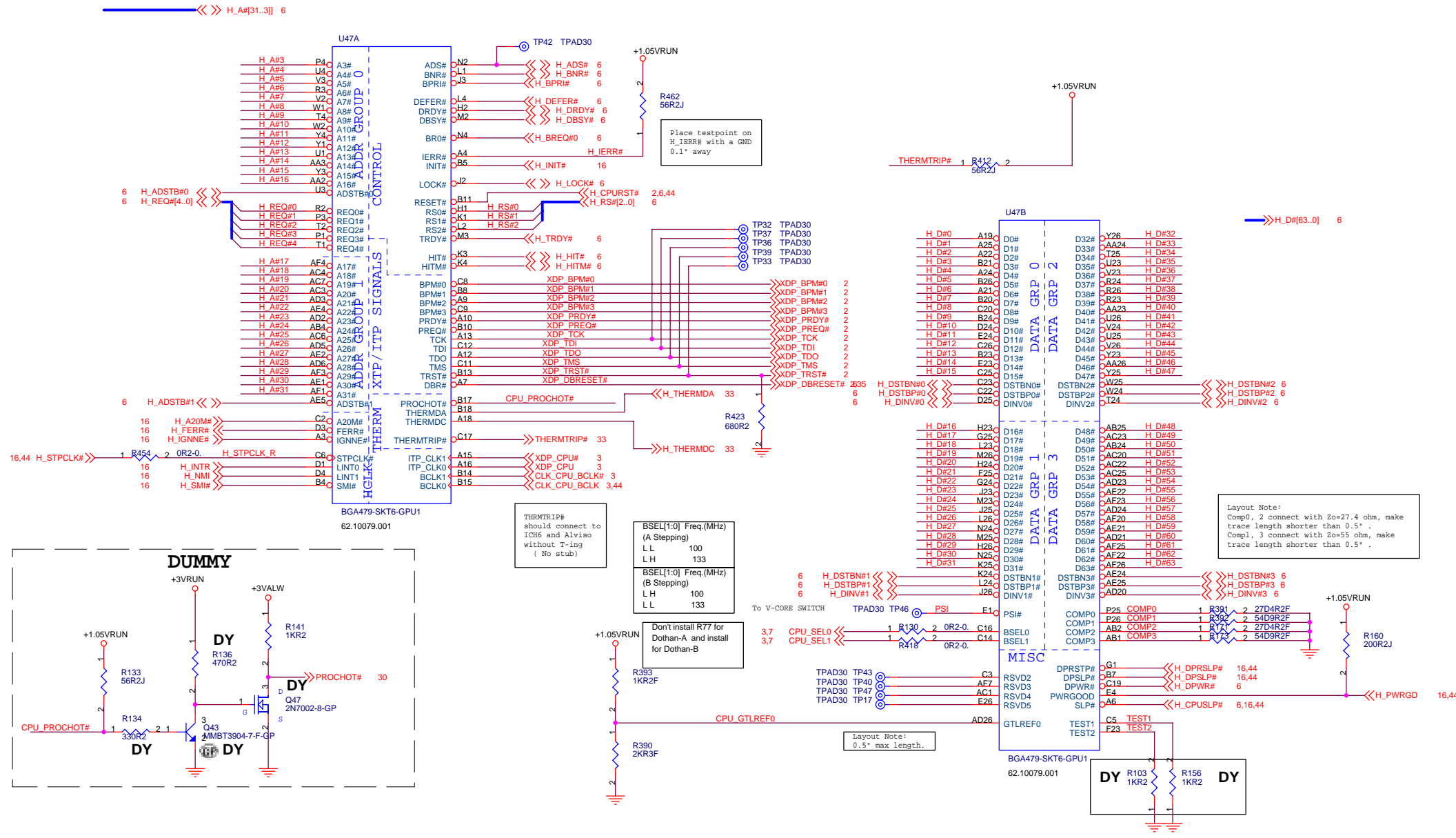
+5VALW	+5VALW	14,30,36,39,43,44
+3VALW	+3VALW	4,14,20,22,29,30,31,33,34,39,43,44
+2.5VRUN	+2.5VRUN	7,9,14,15,18,36,43,44
+5VRUN	+5VRUN	14,15,18,20,21,26,28,30,33,34,36,38,43,44
+12V	+12V	14,23,33,36,43,44
+1.5VRUN	+1.5VRUN	5,7,9,17,18,20,36,44
VCC_CORE	VCC_CORE	5,36,38,44
+1.05VRUN	+1.05VRUN	3,4,5,6,7,9,10,16,18,33,36,40,44
LCDVDD	LCDVDD	14,44
+3VRUN	+3VRUN	3,4,9,11,12,14,15,17,18,19,20,21,22,23,26,27,28,29,30,32,33,35,36,38,43,44

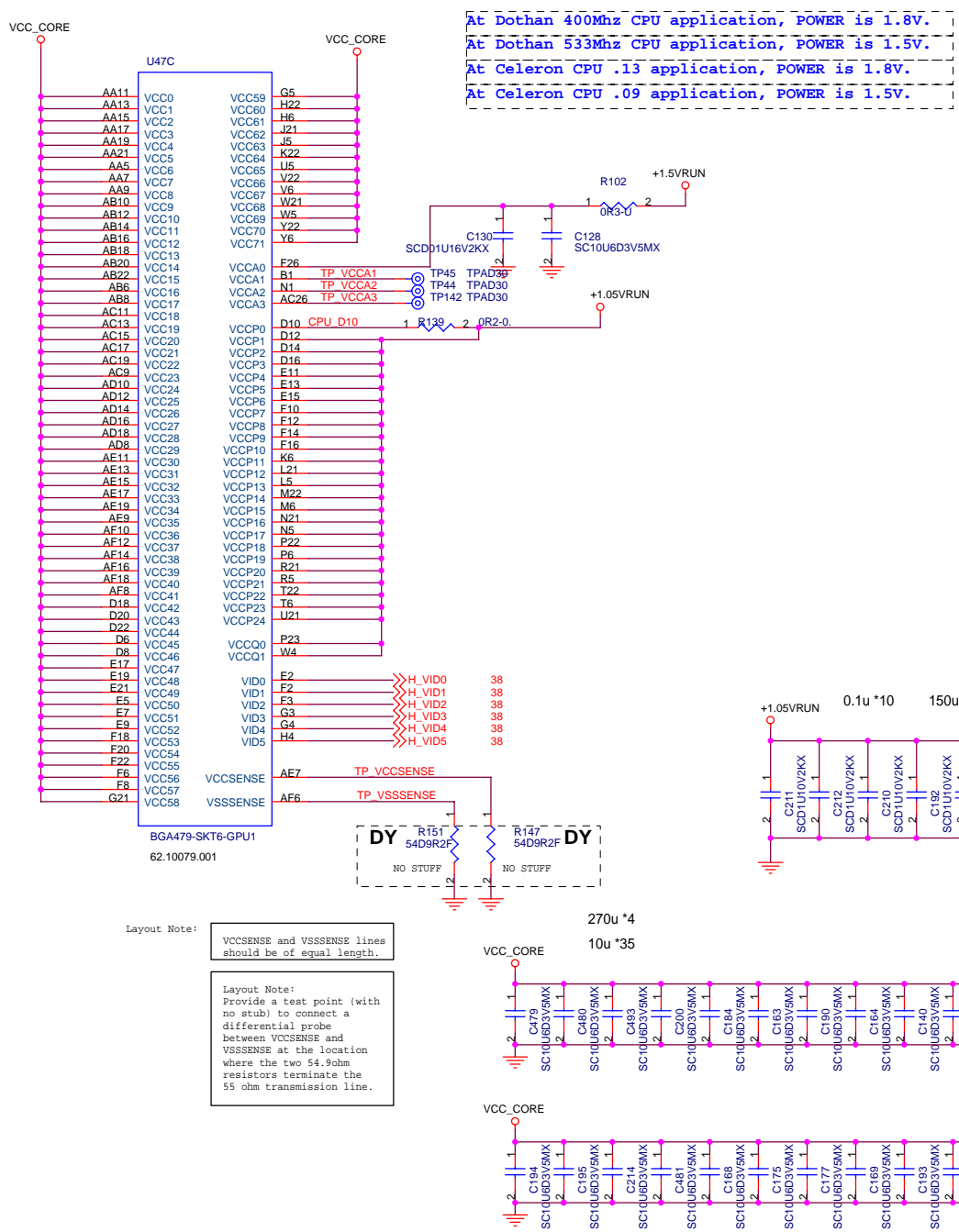


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Title			ITP CONN/Table Of Content		
Size	Document Number			Rev	
A3			Barbados	SD	
Date:	Wednesday, May 18, 2005	Sheet	2	of	44



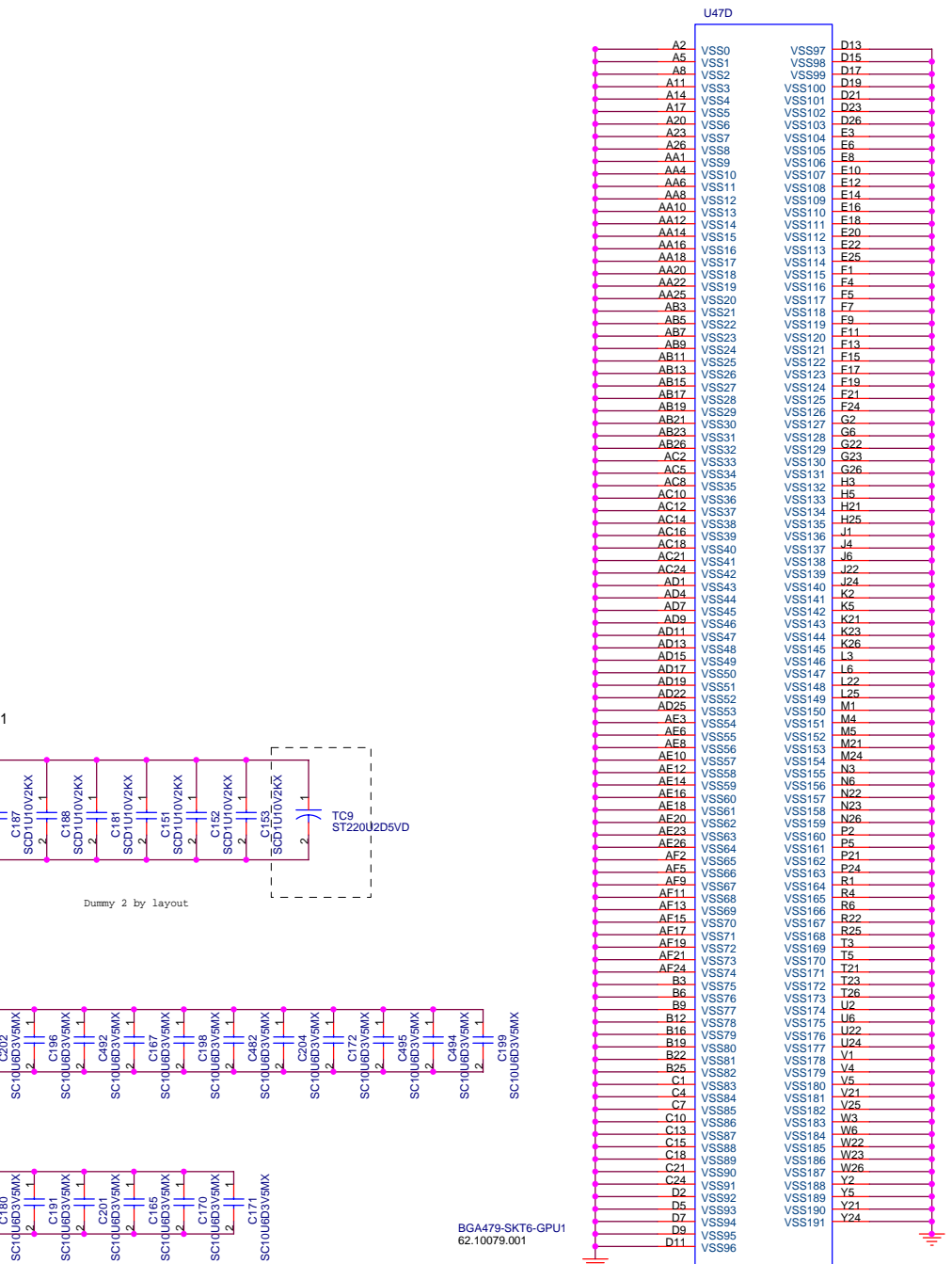


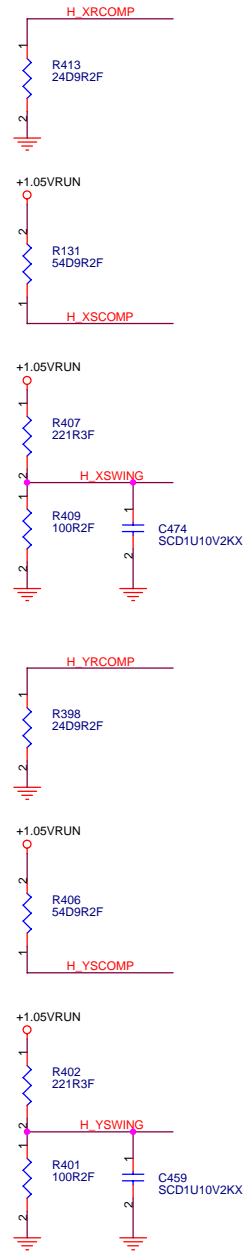


At Dothan 400Mhz CPU application, POWER is 1.8V.
At Dothan 533Mhz CPU application, POWER is 1.5V.
At Celeron CPU .13 application, POWER is 1.8V.
At Celeron CPU .09 application, POWER is 1.5V.

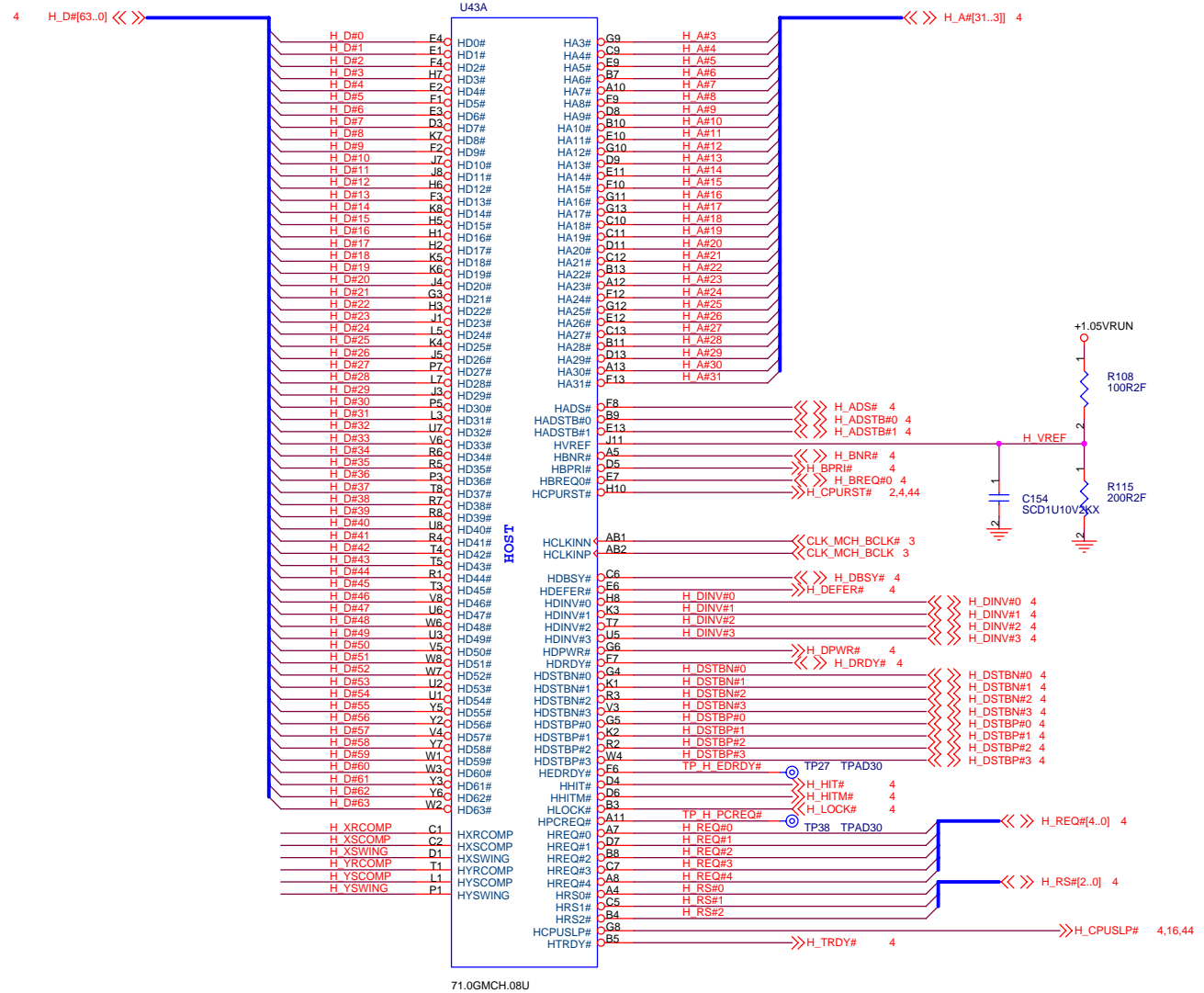
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

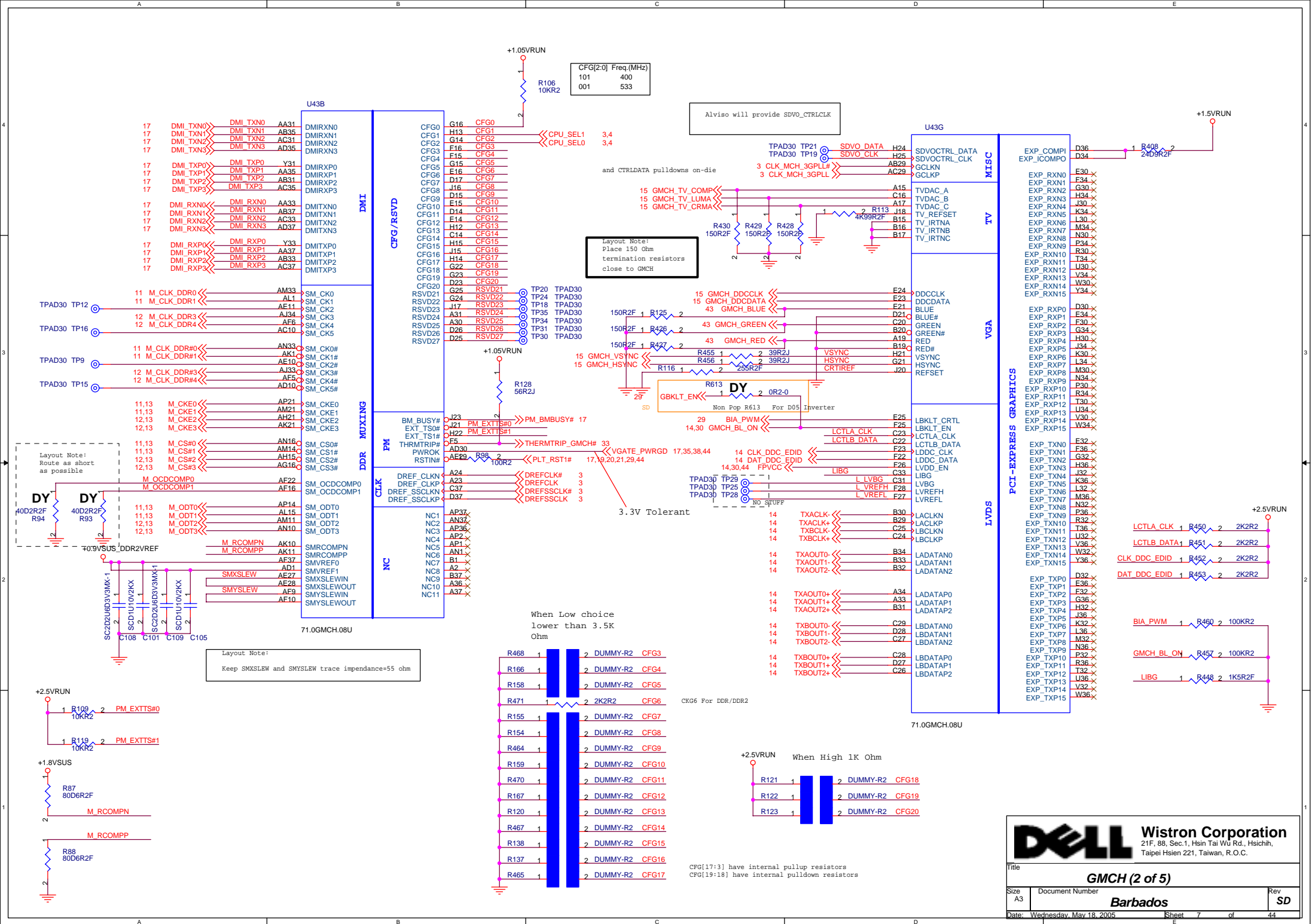
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

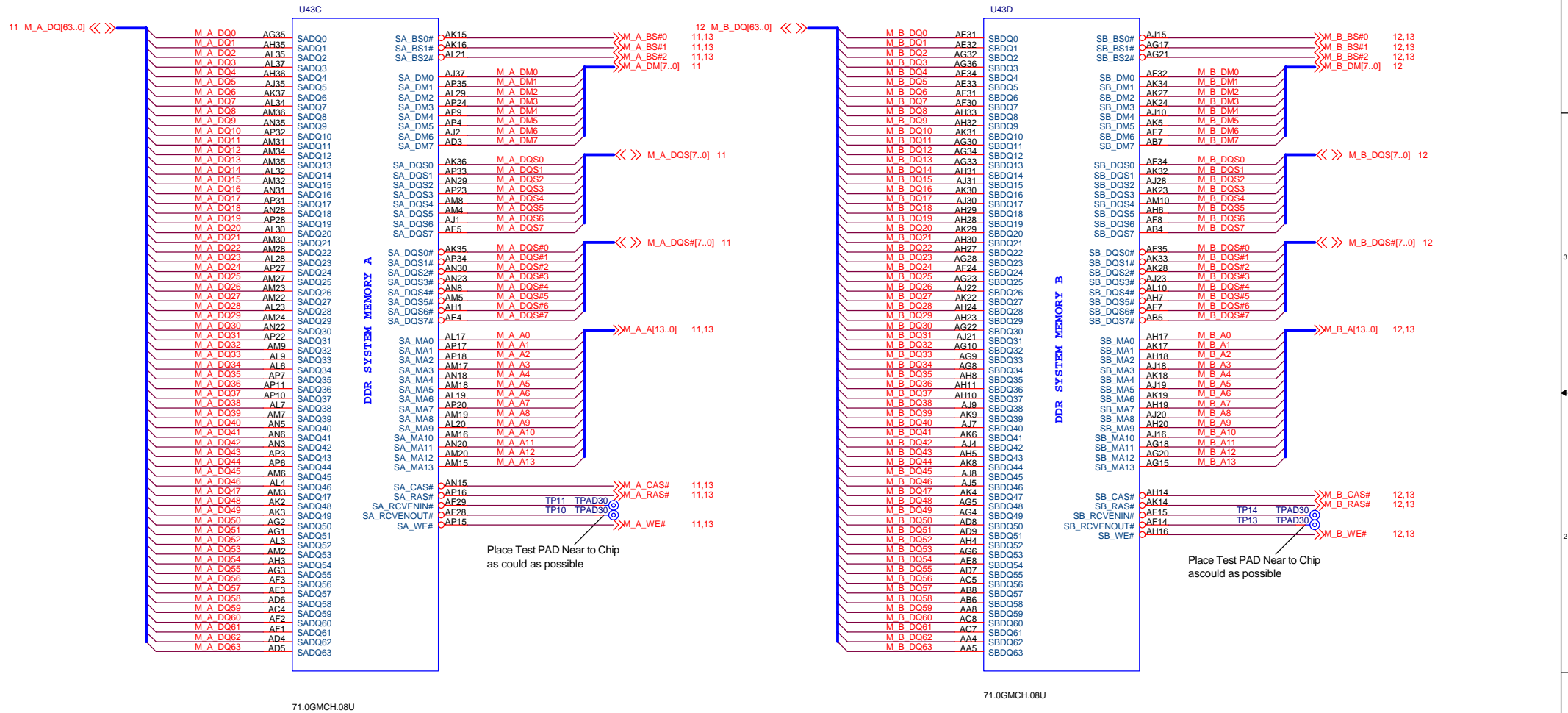


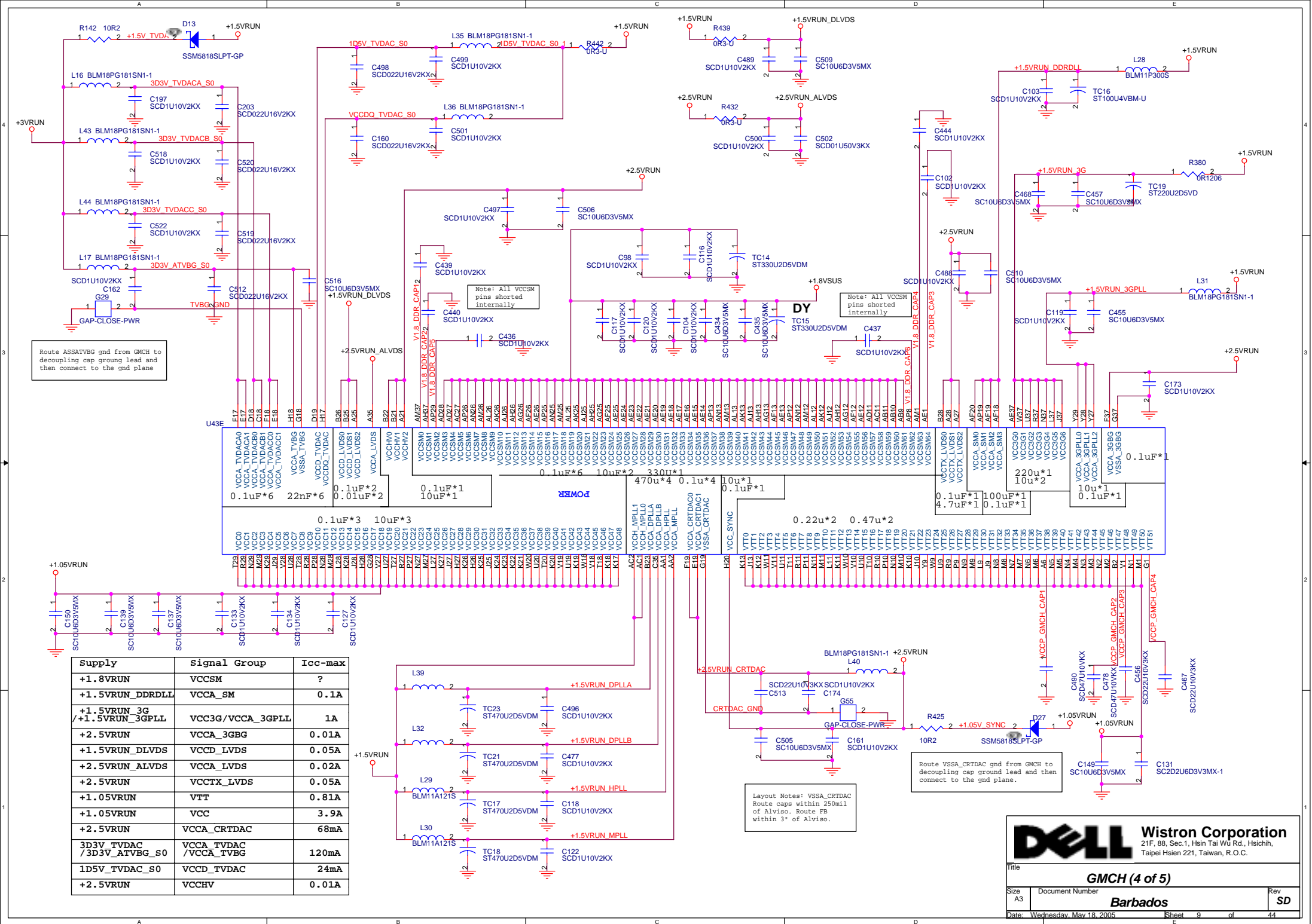


Place them near to the chip



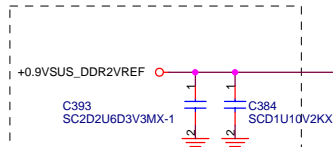








Please close to Pin 1 as close as possible



7,13 M_CS#0 >>> 110C
7,13 M_CS#1 >>> 115C
7,13 M_CKE0 >>> 79
7,13 M_CKE1 >>> 80
8,13 M_A_RAS# >>> 108C
8,13 M_A_CAS# >>> 113C
8,13 M_A_WE# >>> 109C

3,12,19 SMB_C_I<H> >>> 197
3,12,19 SMB_D_I<H> >>> 195

7,13 M_ODT0 >>> 114
7,13 M_ODT1 >>> 119

1 VREF
201 GND

8,13 M_A_A[13..0] <<< >>> M_A_A0 102
M_A_A1 101
M_A_A2 100
M_A_A3 99
M_A_A4 98
M_A_A5 97
M_A_A6 94
M_A_A7 92
M_A_A8 93
M_A_A9 91
M_A_A10 105
M_A_A11 90
M_A_A12 89
M_A_A13 116
X 86 A13
X 84 A14
X 85 A15
A16_BA2

8,13 M_A_BS#2 >>> 107
8,13 M_A_BS#0 >>> 106
8,13 M_A_BS#1 >>> 106

8 M_A_DQ[63..0] <<< >>> M_A_DQ0 5
M_A_DQ1 7
M_A_DQ2 17
M_A_DQ3 19
M_A_DQ4 4
M_A_DQ5 6
M_A_DQ6 14
M_A_DQ7 16
M_A_DQ8 23
M_A_DQ9 25
M_A_DQ10 35
M_A_DQ11 37
M_A_DQ12 20
M_A_DQ13 22
M_A_DQ14 38
M_A_DQ15 43
M_A_DQ16 45
M_A_DQ17 57
M_A_DQ18 44
M_A_DQ19 46
M_A_DQ20 56
M_A_DQ21 58
M_A_DQ22 61
M_A_DQ23 63
M_A_DQ24 73
M_A_DQ25 62
M_A_DQ26 64
M_A_DQ27 74
M_A_DQ28 76
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M_A_DQ40 153
M_A_DQ41 140
M_A_DQ42 142
M_A_DQ43 152
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M_A_DQ47 173
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M_A_DQ56 191
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M_A_DQ60 194
M_A_DQ61 196
M_A_DQ62 197
M_A_DQ63 198

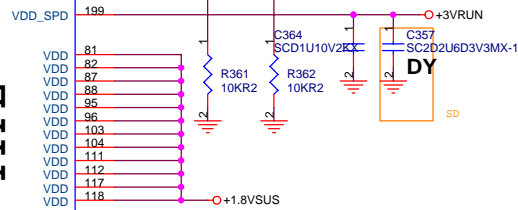
X 50 NC#50
X 69 NC#69
X 83 NC#83
X 120 NC#120
X 163 NC#163/TEST

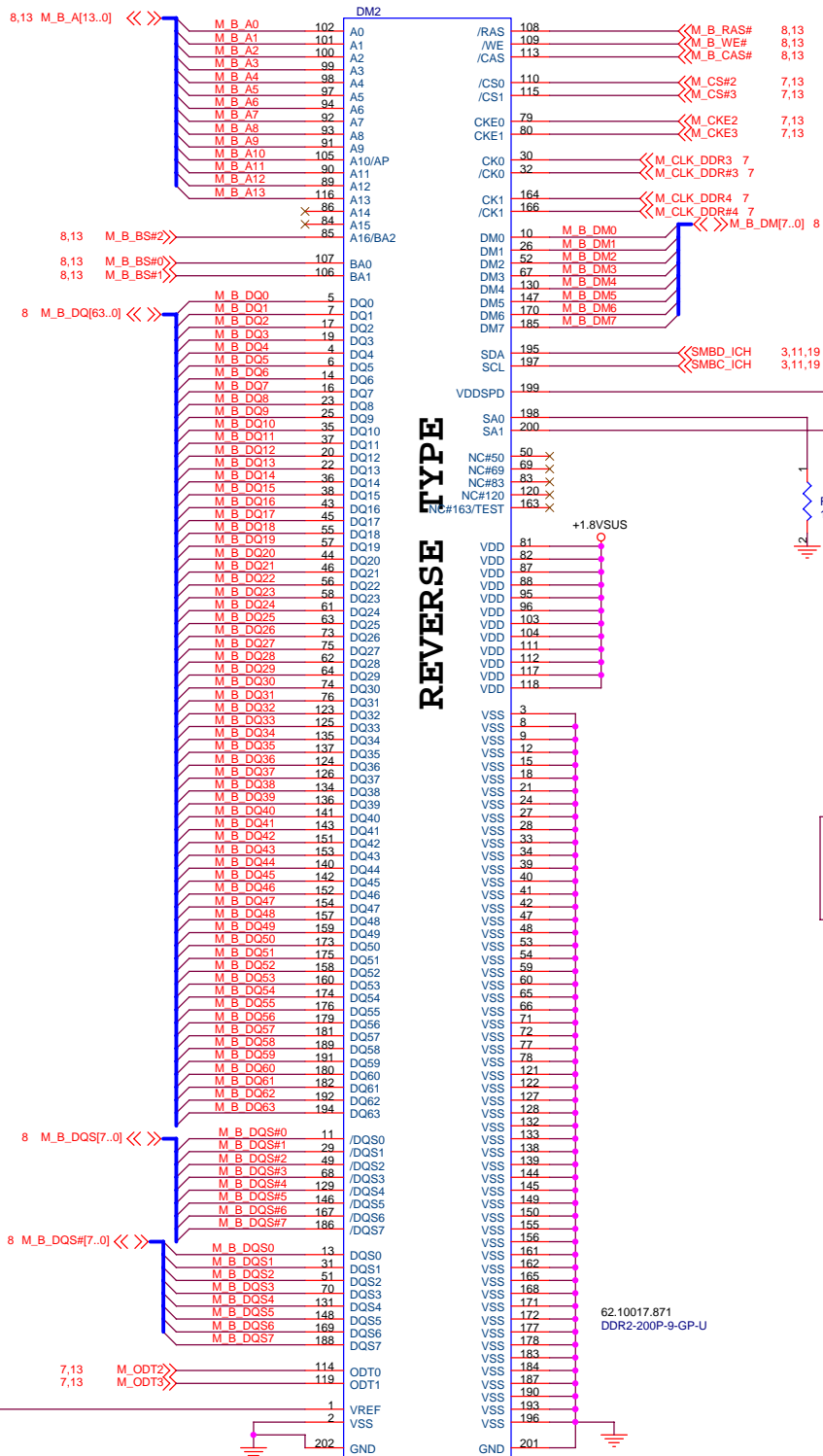
NORMAL TYPE

MH2 >>> M_A_DQS0 13
M_A_DQS1 31
M_A_DQS2 51
M_A_DQS3 70
M_A_DQS4 131
M_A_DQS5 148
M_A_DQS6 169
M_A_DQS7 188
M_A_DQS#0 11
M_A_DQS#1 29
M_A_DQS#2 49
M_A_DQS#3 68
M_A_DQS#4 129
M_A_DQS#5 146
M_A_DQS#6 167
M_A_DQS#7 186

10 M_A_DM0 >>> M_A_DM[7..0] 8
26 M_A_DM1 >>> 52 M_A_DM2 >>> 67 M_A_DM3 >>> 130 M_A_DM4 >>> 147 M_A_DM5 >>> 170 M_A_DM6 >>> 185 M_A_DM7 >>>

CK0 >>> M_CLK_DDR0 7
CK0# >>> M_CLK_DDR#0 7
CK1 >>> M_CLK_DDR1 7
CK1# >>> M_CLK_DDR#1 7





REVERSE TYPE

Place one cap to each power pin and as close as possible

Use +0.9VVRUN or +0.9VSUS_DDR2VREF

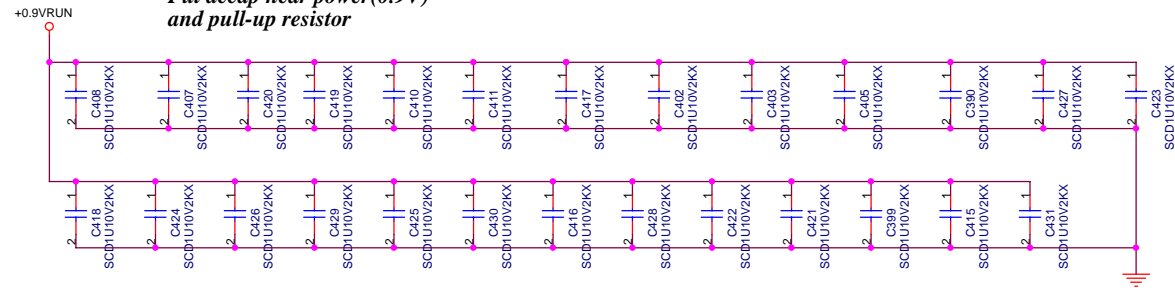
Please close to Pin 1 as close as possible

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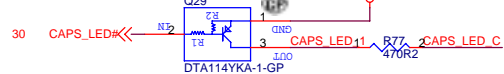
Title DDR-2 SO-DIMM B		
Size A3	Document Number Barbados	Rev SD
Date: Wednesday, May 18, 2005	Sheet 12 of	44

Decoupling Capacitor

*Put decap near power(0.9V)
and pull-up resistor*



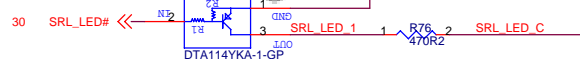
CAP LED



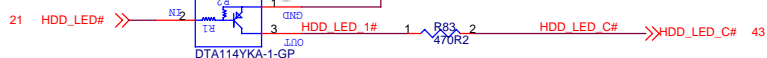
NUM LED



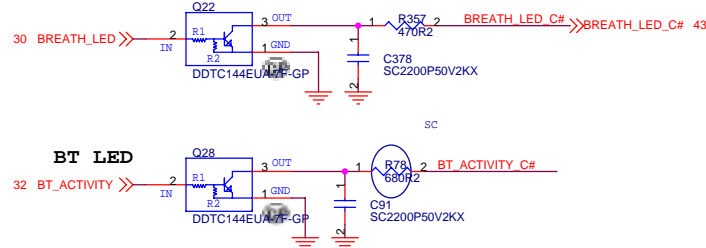
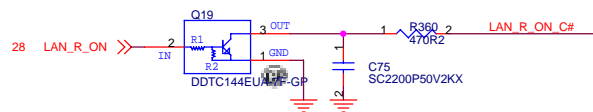
SCR LED



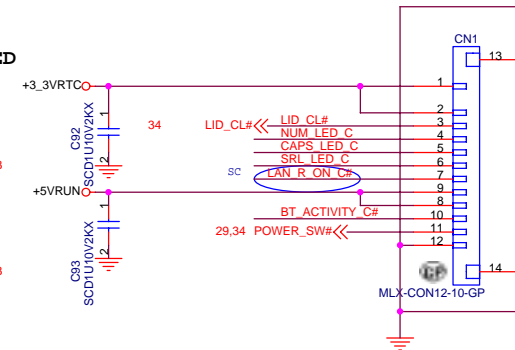
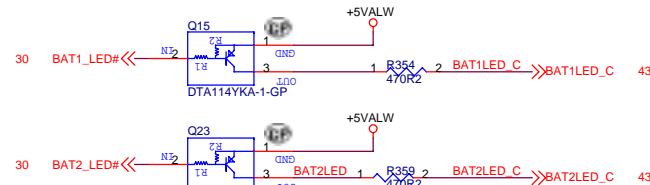
HDD LED



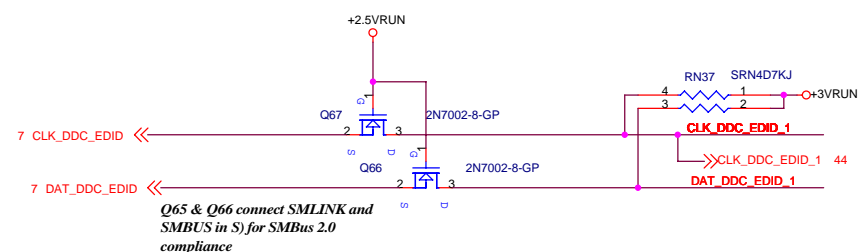
WIRLESS LED



HDD / BT / CAP / NUM / SCR LED POWER LED

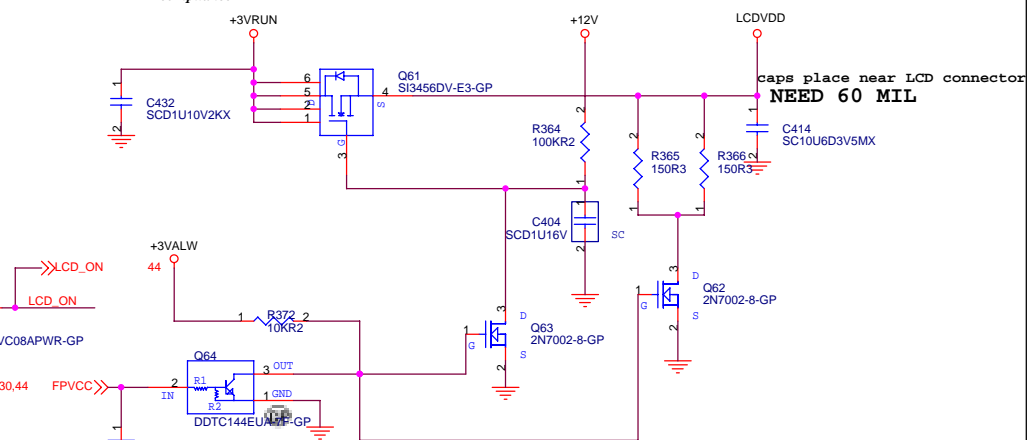


SMBUS



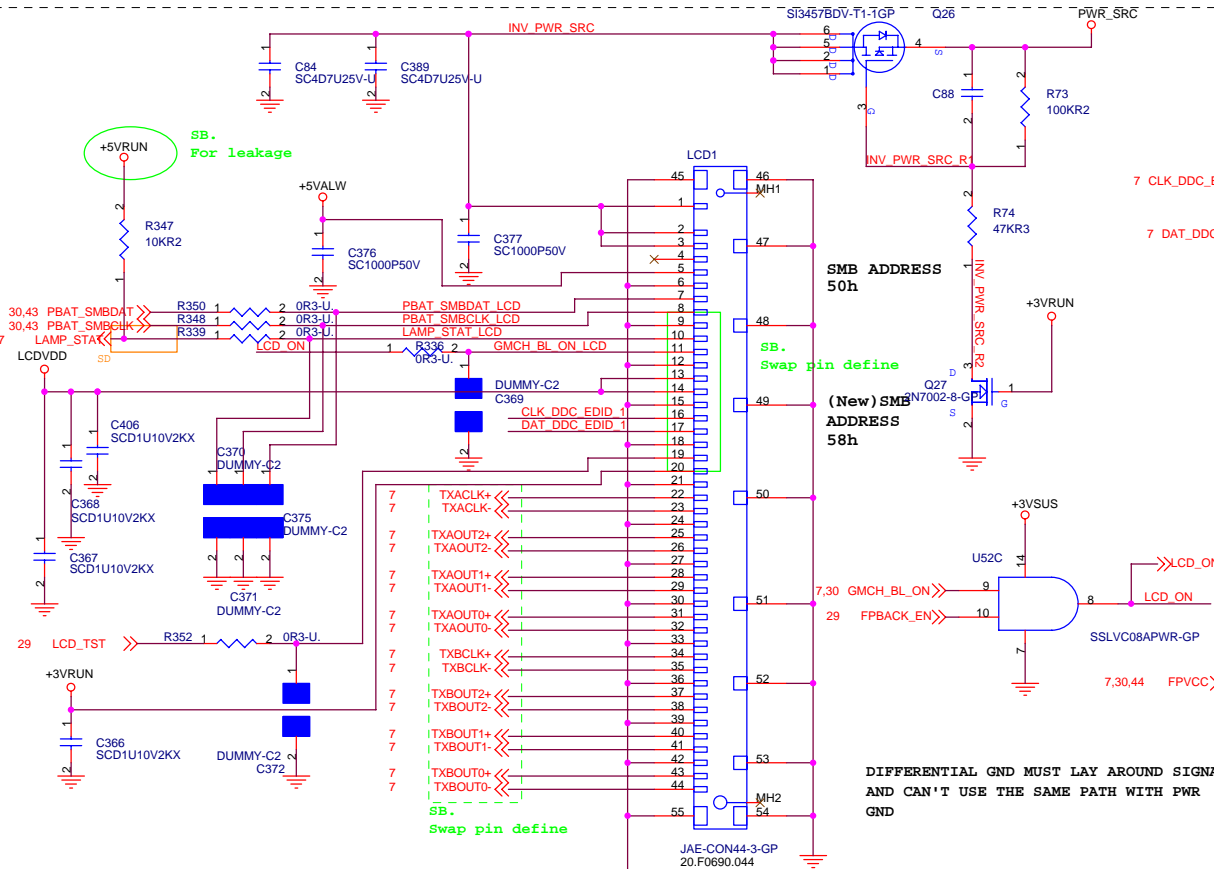
Q65 & Q66 connect SMLINK and SMBUS in S for SMBUS 2.0 compliance

caps place near LCD connector
NEED 60 MIL

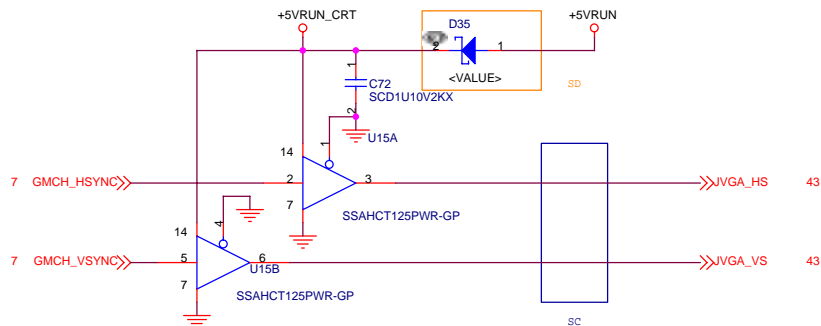


DIFFERENTIAL GND MUST LAY AROUND SIGNAL
AND CAN'T USE THE SAME PATH WITH PWR
GND

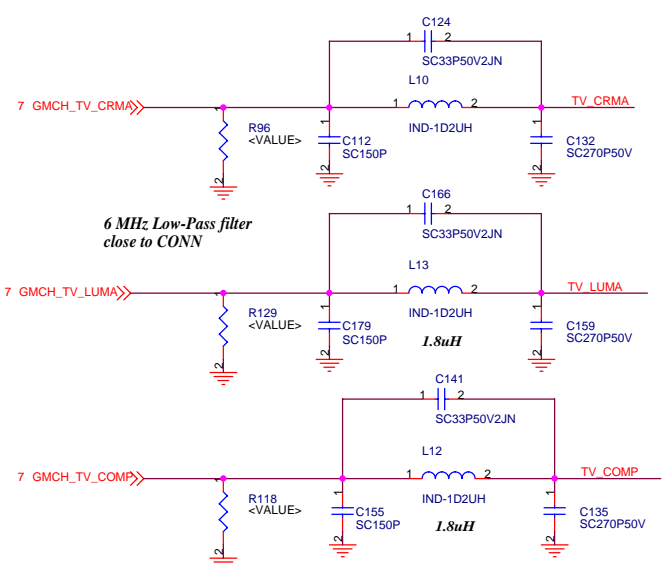
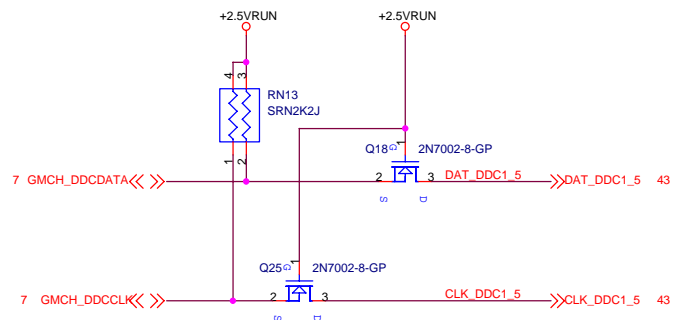
LCD/INVERTER CONN



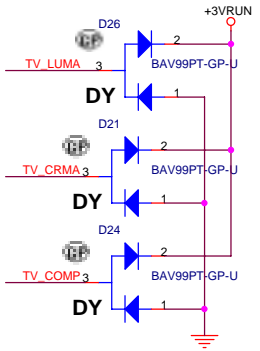
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title LCD_INVERTER & LED		
Size A3	Document Number Barbados	Rev SD
Date: Wednesday, May 18, 2005	Sheet 14	of 44



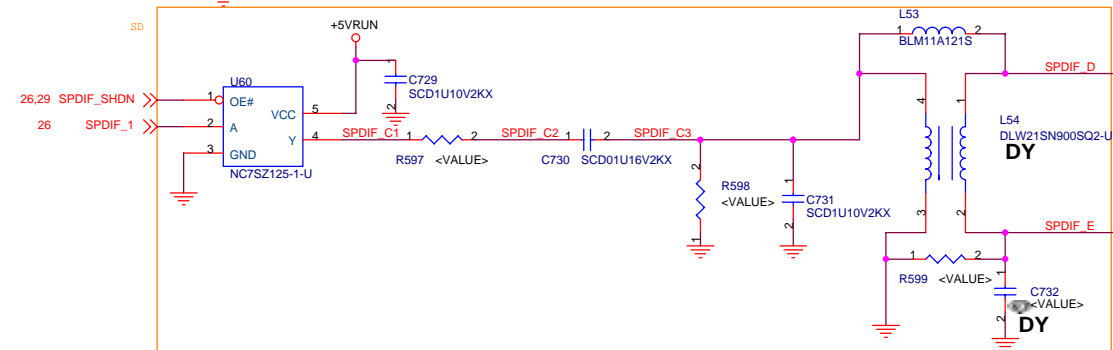
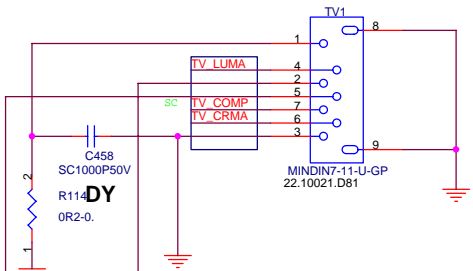
DDC_CLK & DATE LEVEL SHIFT



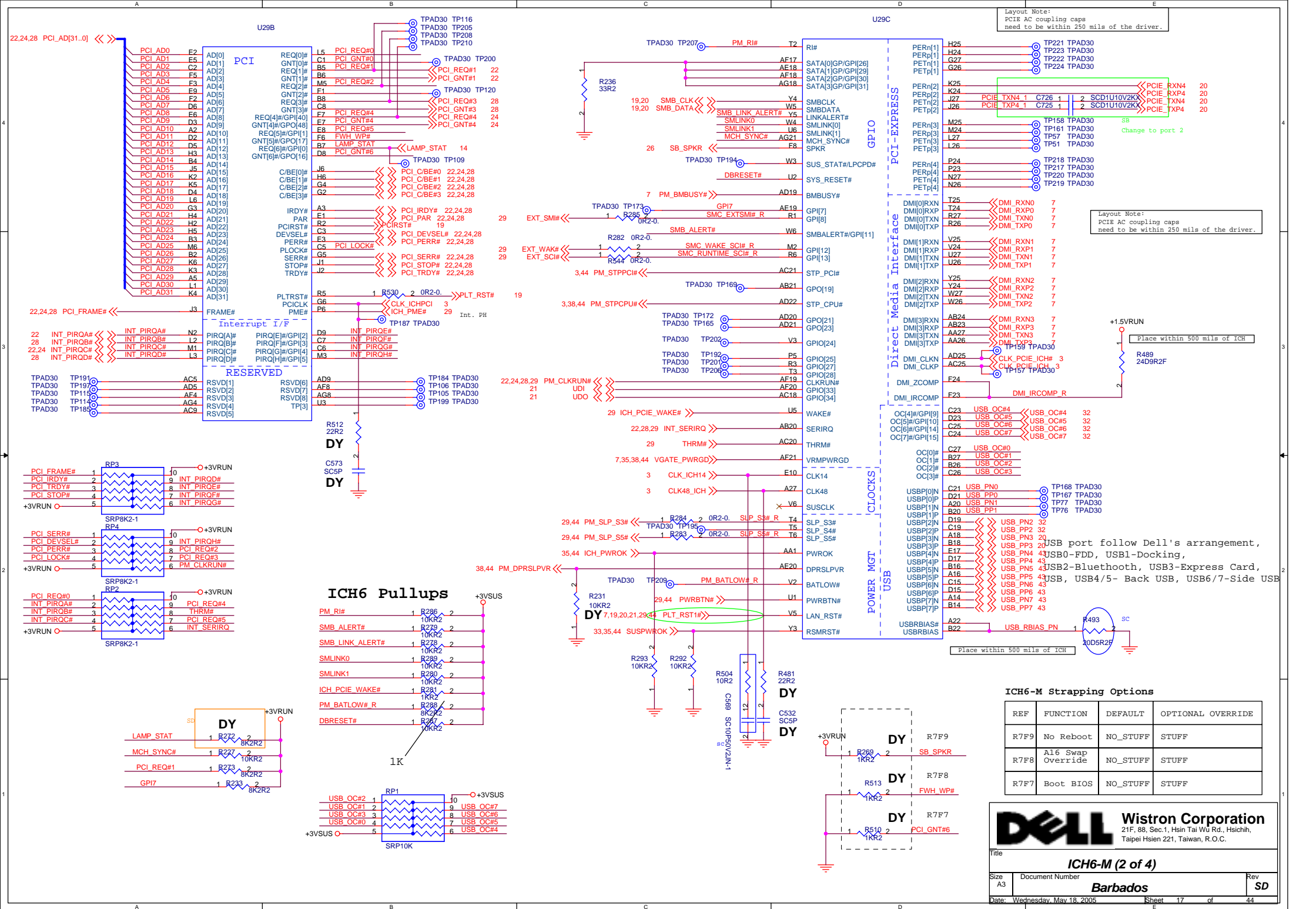
ESD Protection Diode



TVOUT CONN



Title		TV CONN.	
Size	Document Number	Rev	SD
A3		Barbados	
Date: Wednesday, May 18, 2005		Sheet	15 of 44



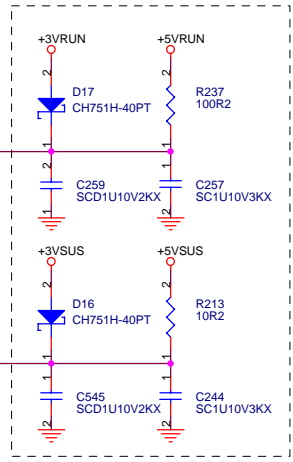
Supply	Signal Group	Icc-max
V5REF_S0	V5REF	0.001A
V5REF_S5	V5REF_SUS	0.01A
+3VRUN	VCC3_3	0.19A
+3VRUN	VCCSUS3_3 /VCCLAN3_3	0.39A
+2.5VRUN	VCC2_5	0.01A
+1.5VRUN	VCC1_5	2.95A
+1.5VSUS	VCCSUS1_5 /VCCLAN1_5	0.27A
+1.05VRUN	V_CPU_IO	0.014A
VCCRTC	VCCRTC	5uA

Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

Layout Note:
Place near pin AA19

ALL NO STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6

*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail



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Title
ICH6-M (3 of 4)

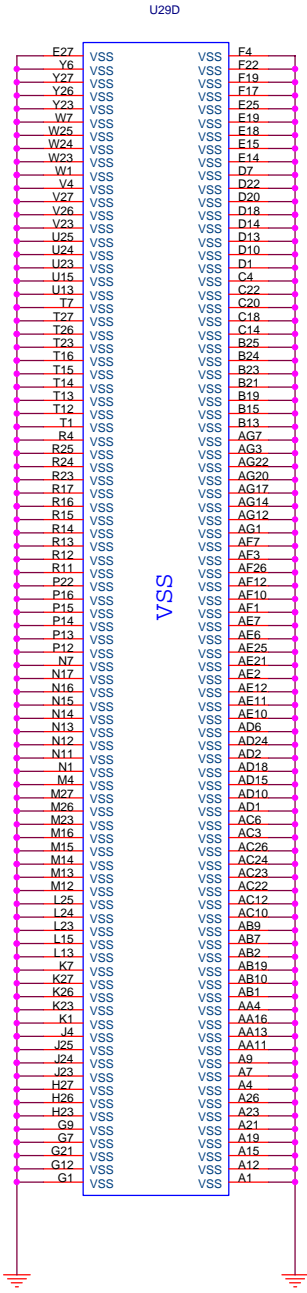
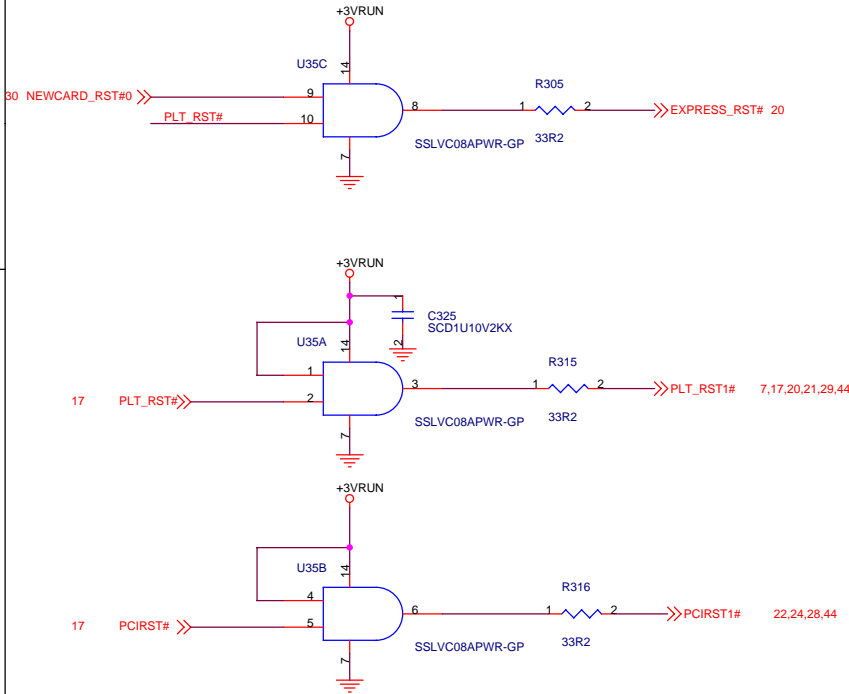
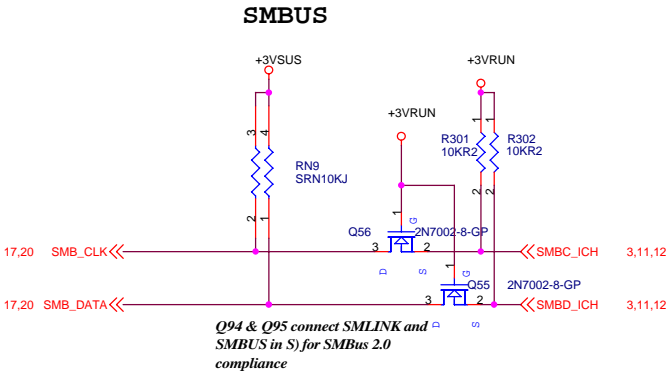
Size
A3

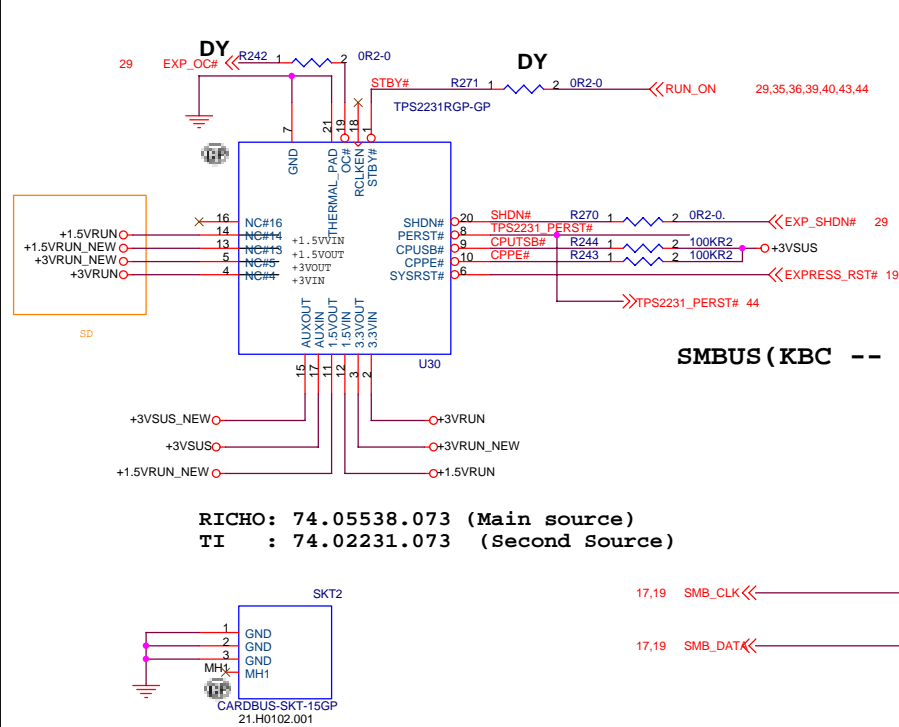
Document Number
Barbados

Rev
SD

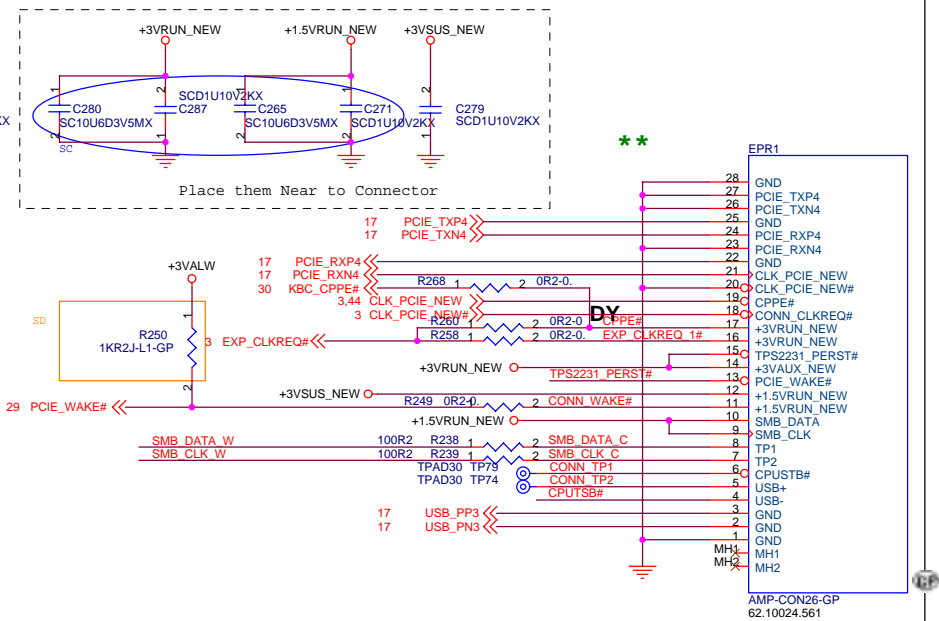
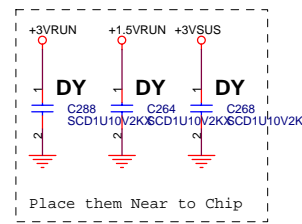
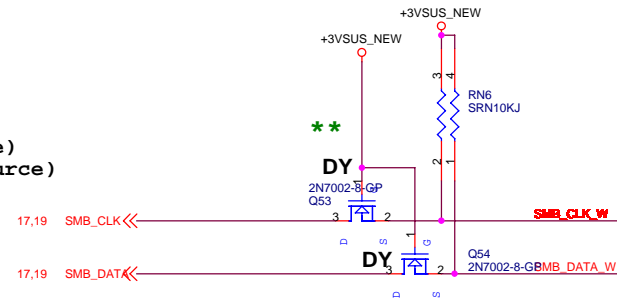
Date: Wednesday, May 18, 2005

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SMBUS (KBC -- NEWCARD, LAN)



Geometry : 102003-6

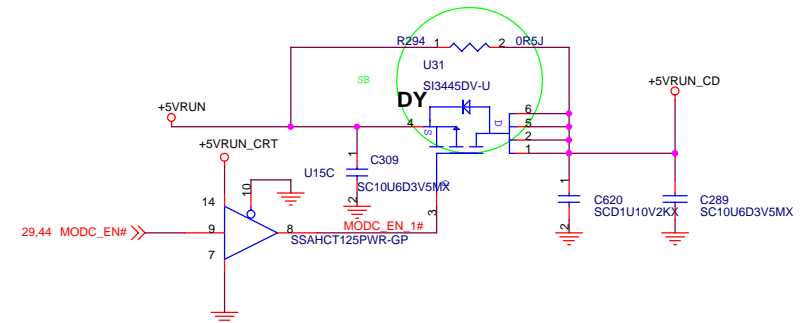
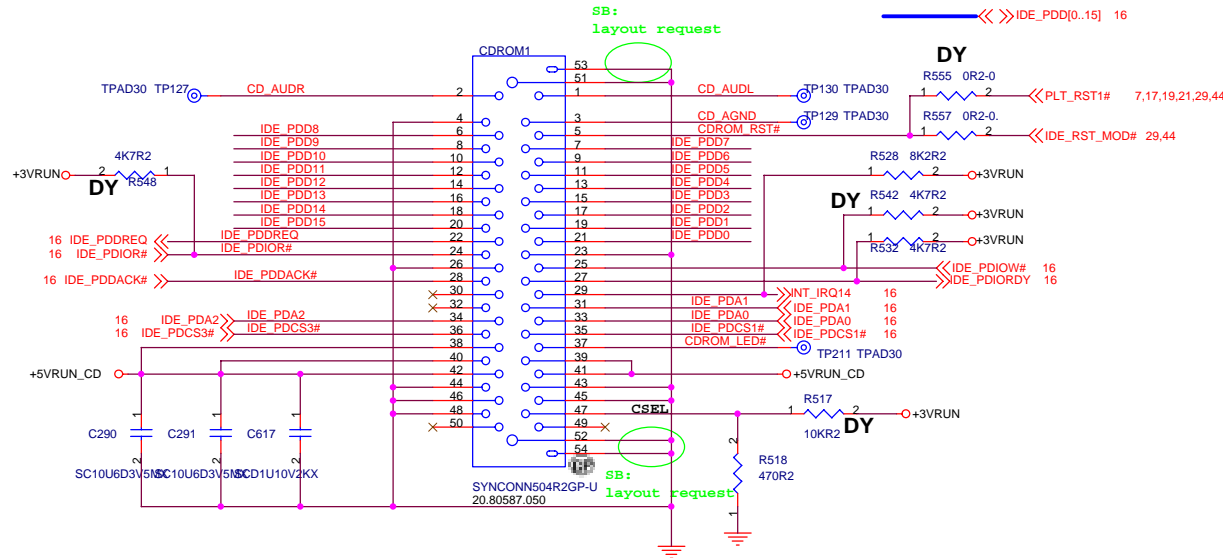


For Newcard socket

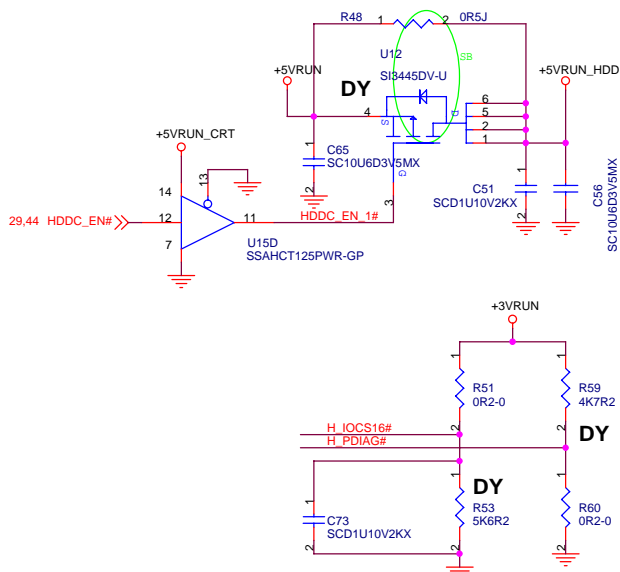
NEWCARD Connector

Reserve the symbol
for TOP side
connector

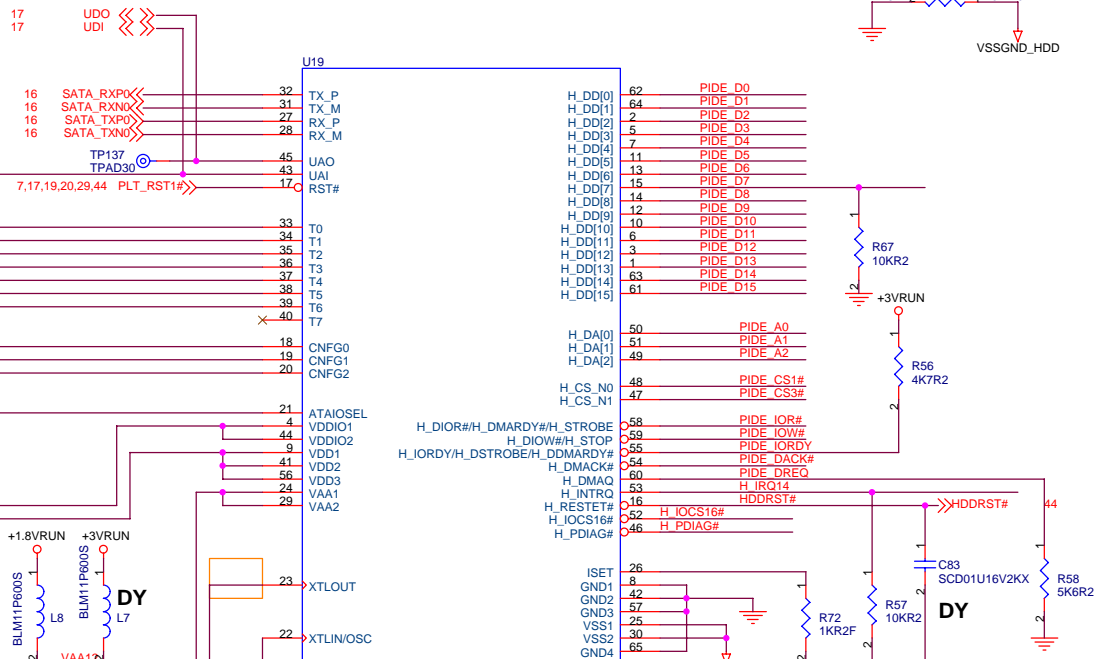
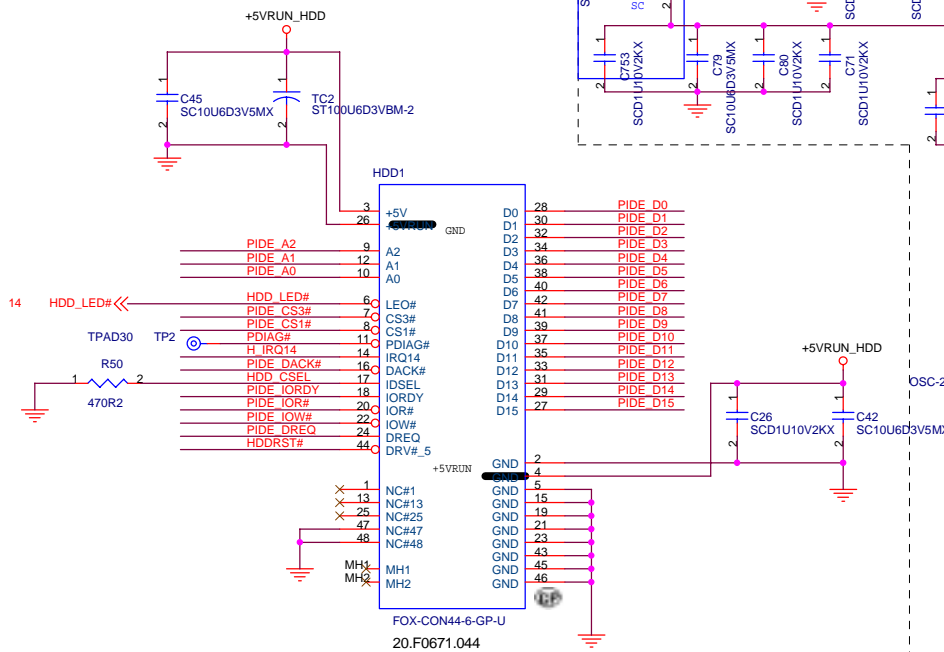
CDROM



HDD power



HDD CONN



S-ATA TABLE 1/2

U19	88SA8040	Si3811
C73	NO_ASM	ASM
L8	NO_ASM	ASM
L7	NO_ASM	ASM
R75	NO_ASM	ASM
R369	NO_ASM	ASM
R66	NO_ASM	ASM
R370	NO_ASM	ASM
R68	NO_ASM	ASM
R363	NO_ASM	ASM
R371	NO_ASM	ASM
R70	NO_ASM	ASM
R64	NO_ASM	ASM

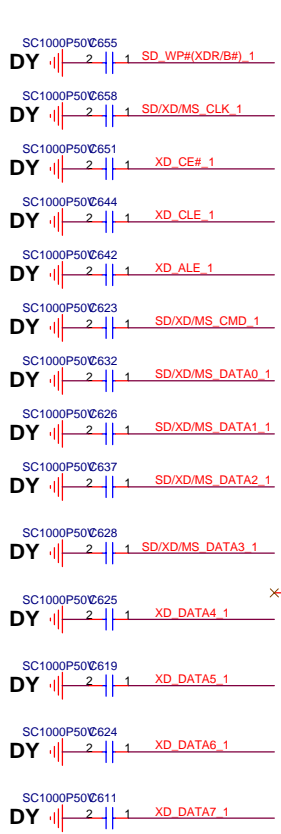
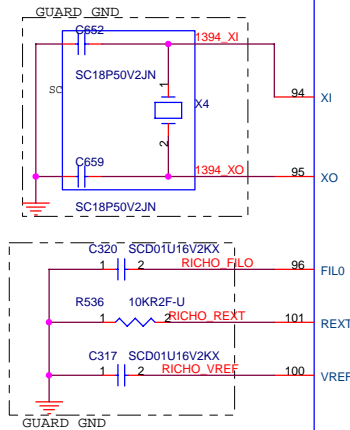
S-ATA TABLE 2/2

U19	88SA8040	Si3811
R71	NO_ASM	NO_ASM
R61	NO_ASM	NO_ASM
R82	NO_ASM	NO_ASM
R72	12.1K	1K
R53	NO_ASM	NO_ASM
R59	NO_ASM	NO_ASM
R60	NO_ASM	NO_ASM
R80	NO_ASM	NO_ASM
R65	NO_ASM	NO_ASM
R81	NO_ASM	NO_ASM
R69	NO_ASM	NO_ASM
R79	NO_ASM	NO_ASM
R51	NO_ASM	NO_ASM
R587	0 ohm	100 ohm
R588	NO_ASM	120 ohm

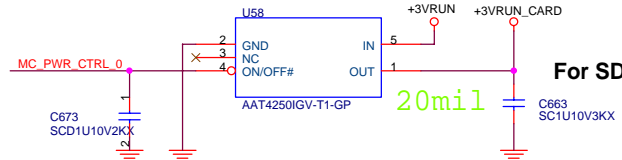
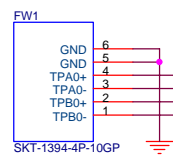
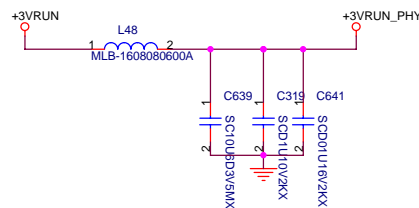
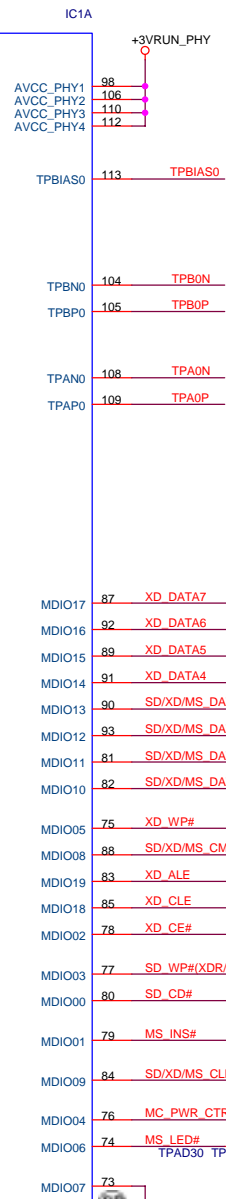
<Variant Name>

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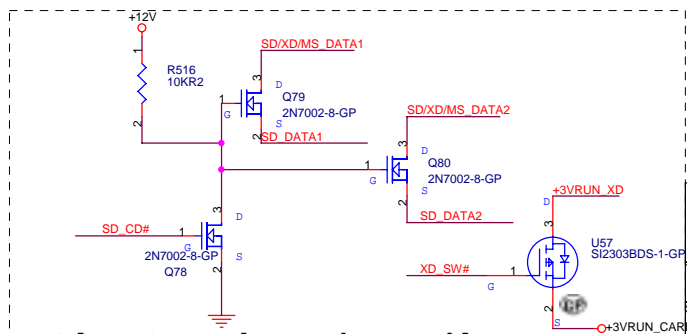
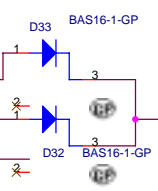
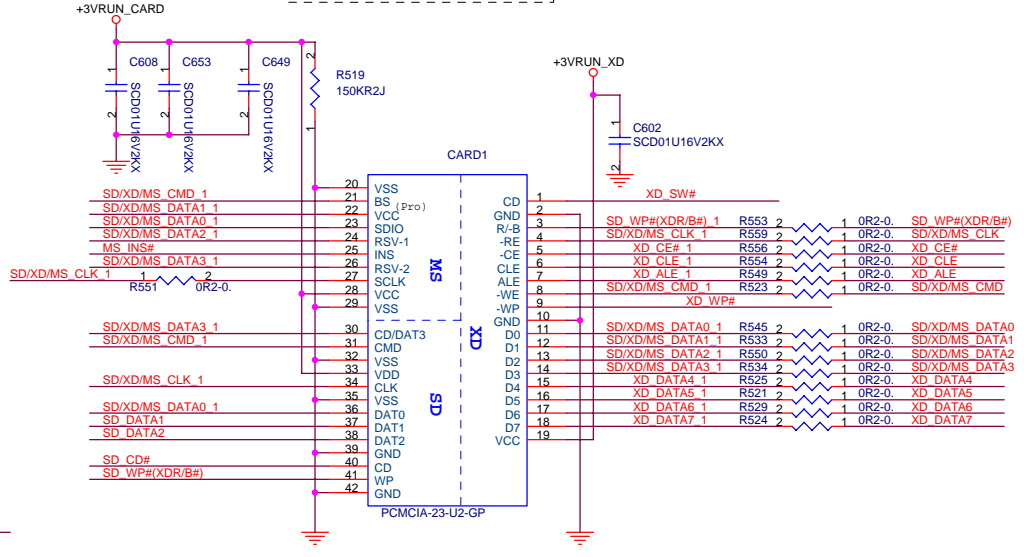
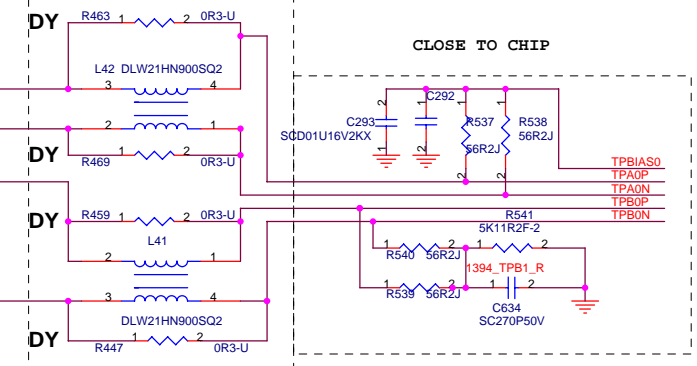
Title		SATA HDD/CD ROM	
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IEEE1394/SD



Reserve R547, R548, R550, R551 for co-layout



DELL Wistron Corporation
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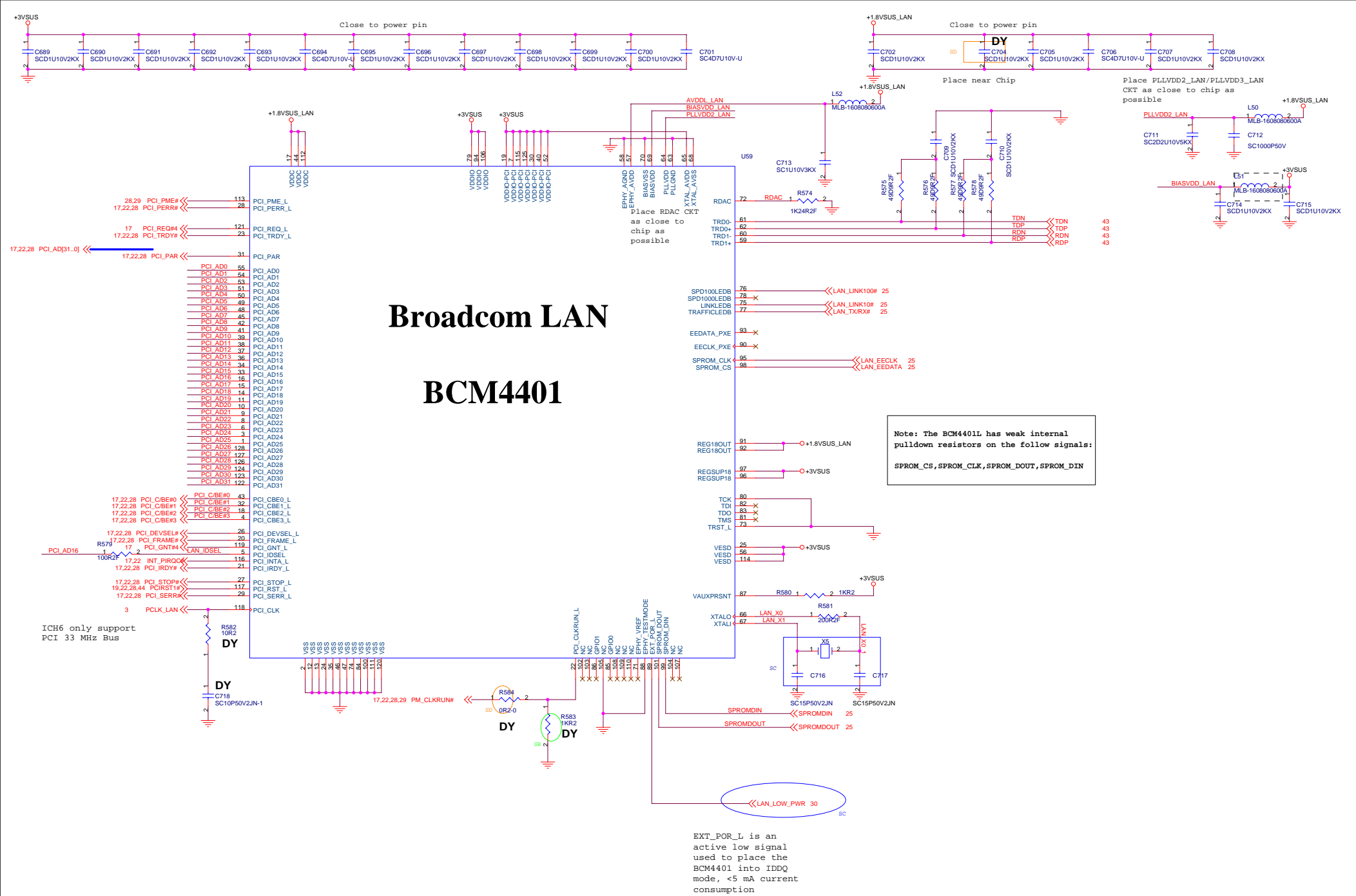
Title: **R5C832_1394_Tin1(2/2)**

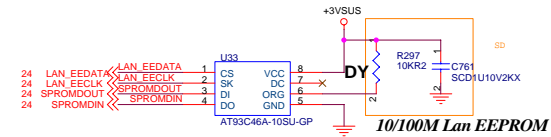
Size: A3 Document Number: **Barbados** Rev: **SD**

Date: Wednesday, May 18, 2005 Sheet: 23 of 44

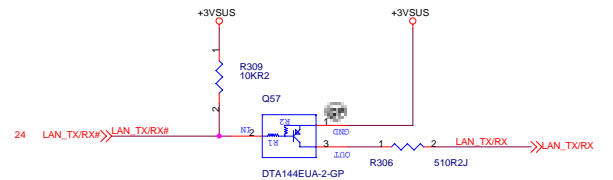
Broadcom LAN

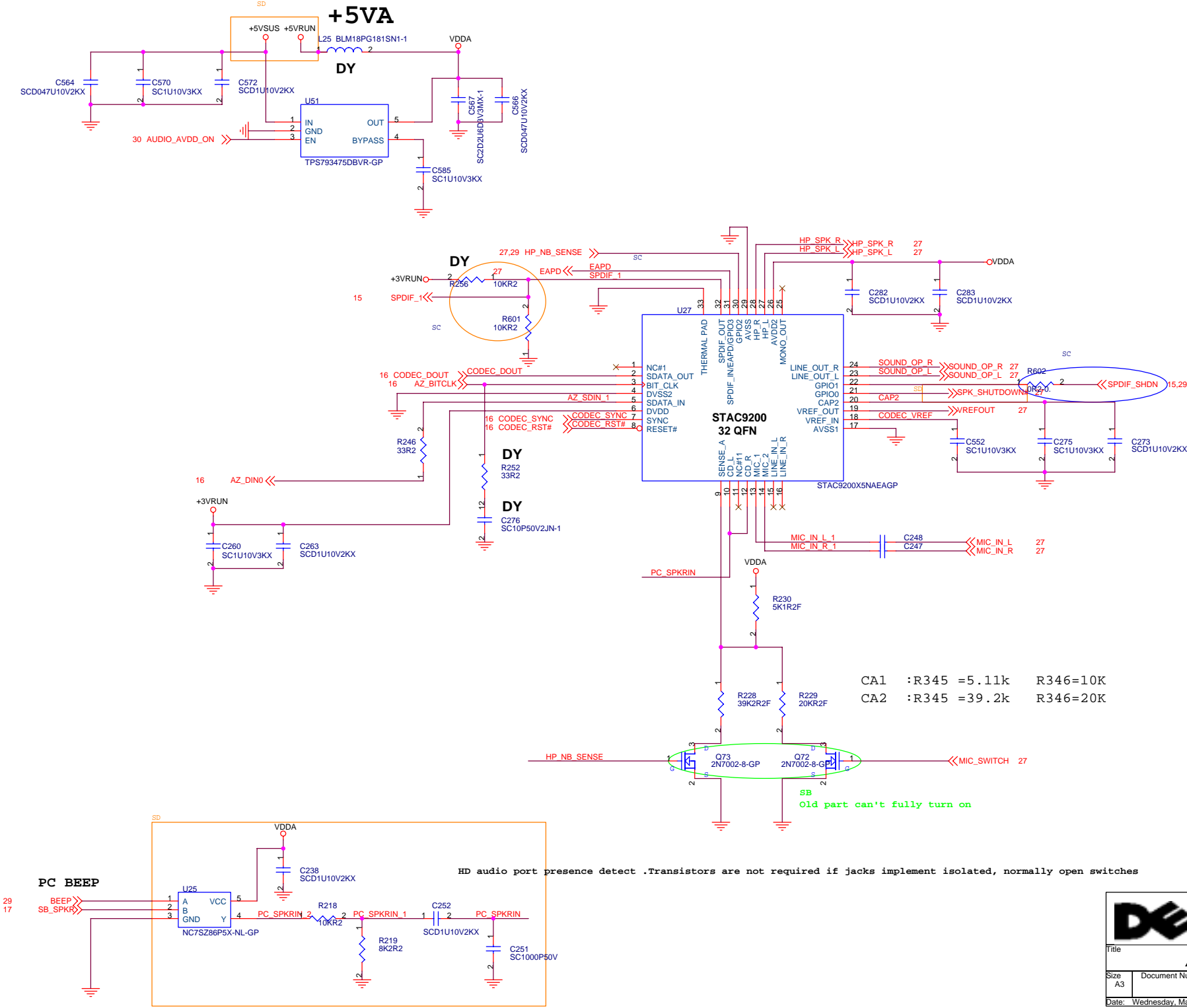
BCM4401

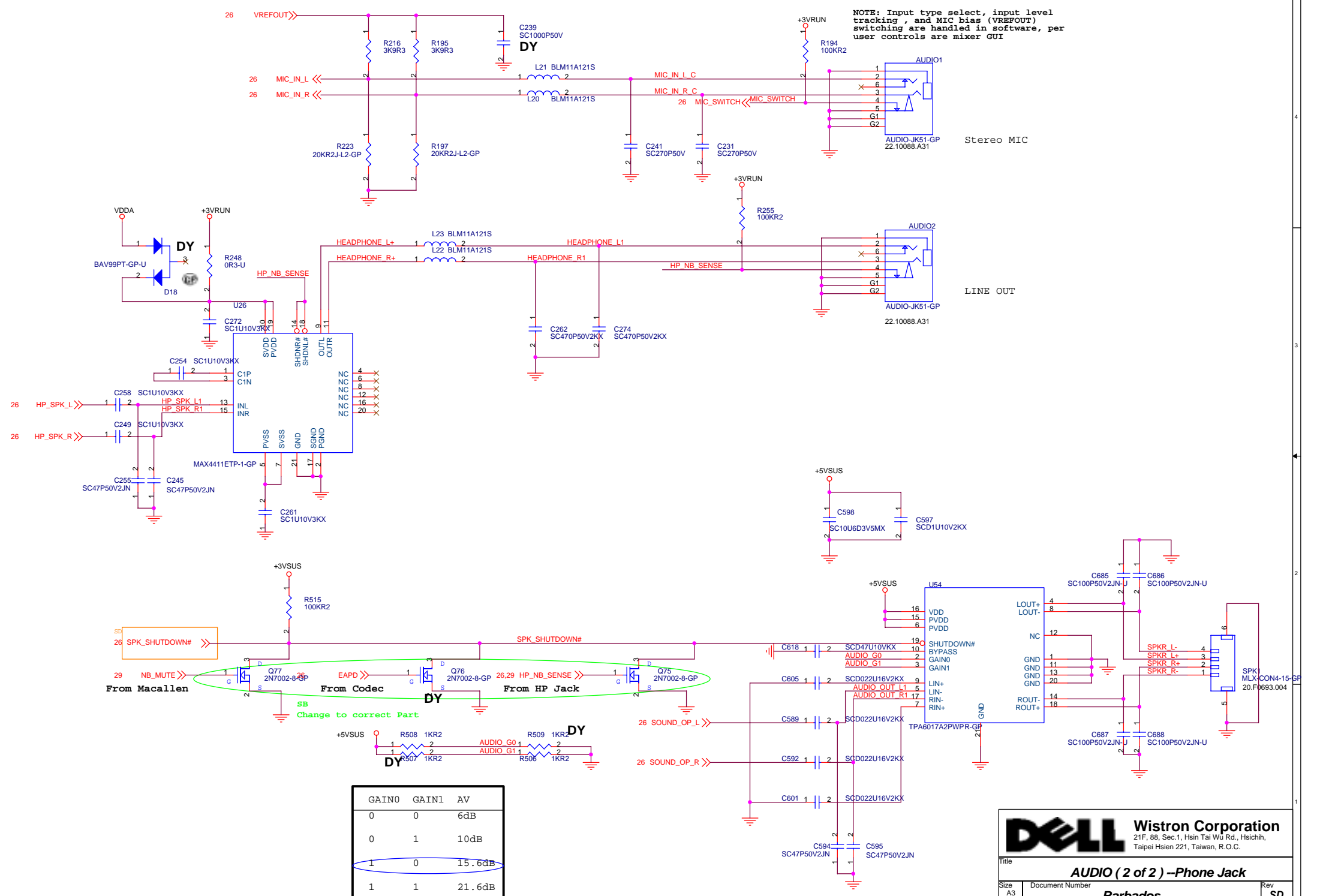





Atmal: AT93C46-10SI "72.93C46.K01" (Main source)
ST : M93C46-W "72.93C46.E01" (2nd source)









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Title

AUDIO (2 of 2) --Phone Jack

Size
A3

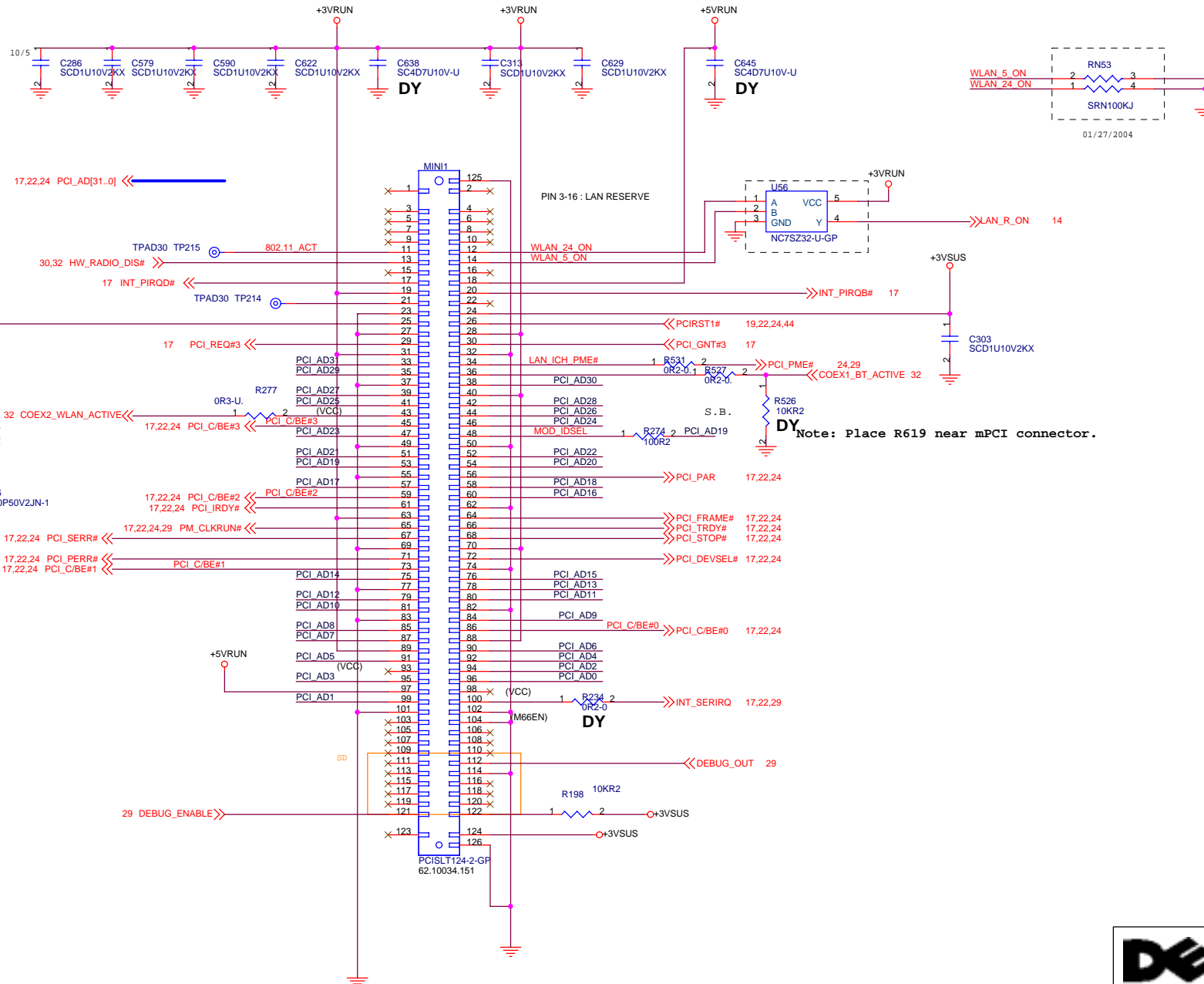
Document Number
Barbados

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SD

Date: Wednesday, May 18, 2005

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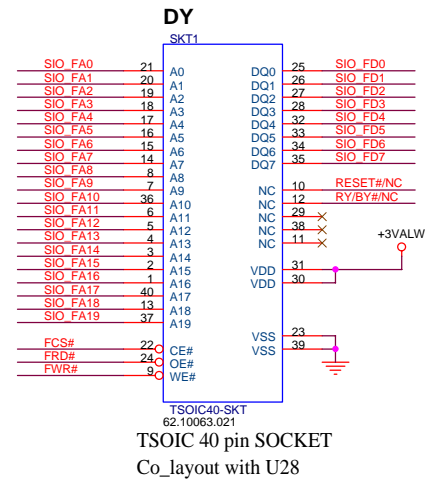
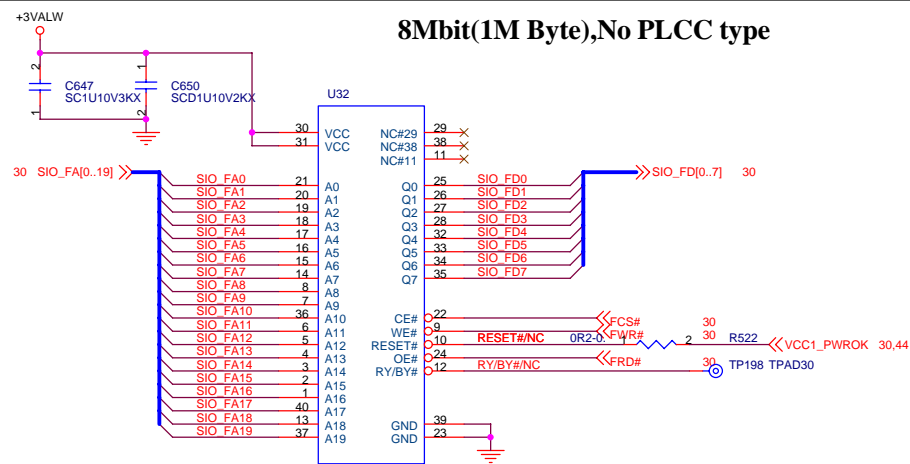
MINI PCI



Note: Place R619 near mPCI connector.



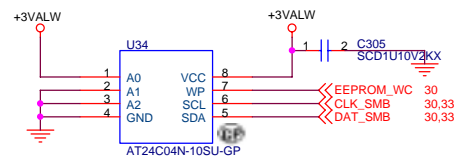
8Mbit(1M Byte),No PLCC type



MXIC: MX29LV008CTTI-90G "72.29008.G09" (Main sorce,LF,bottom boot block)
ST: M29W008AB-90 "72.29008.C09" (2nd sorce)

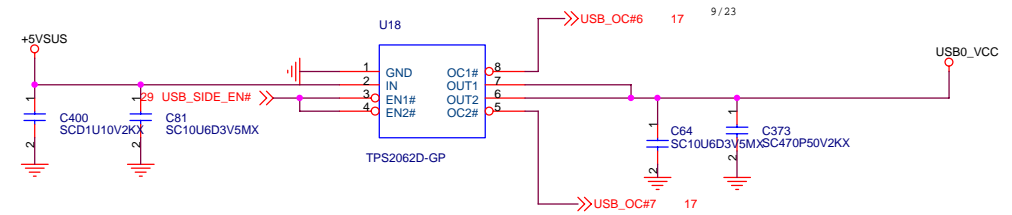
SMBus address A2

User Password

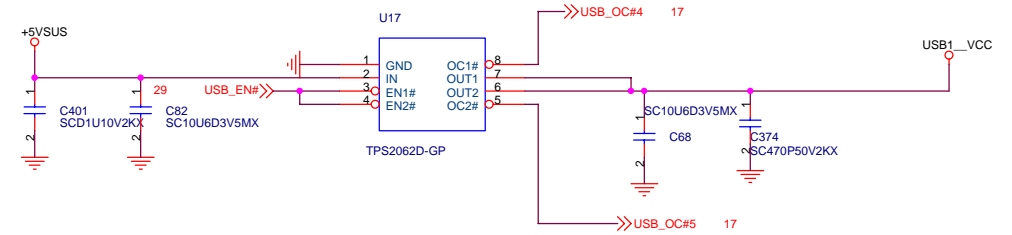


Atmel: AT24C04N-10SI "72.24C04.D01" (Main sorce)
ST : M24C04 "72.24C04.B01" (2nd sorce)

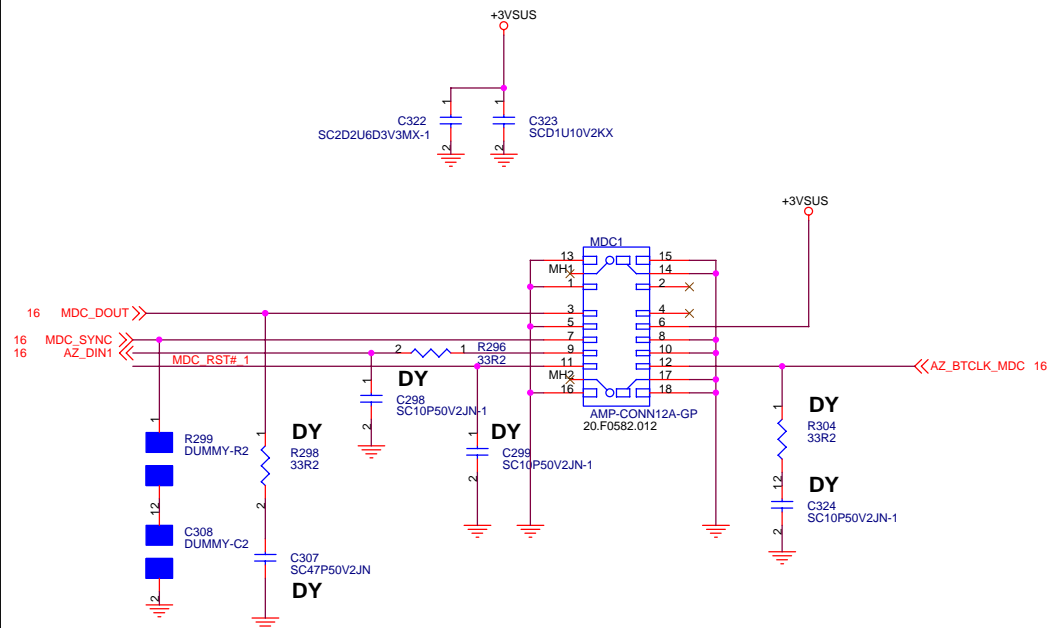
Dual USB0_VCC switch for USB6/USB7



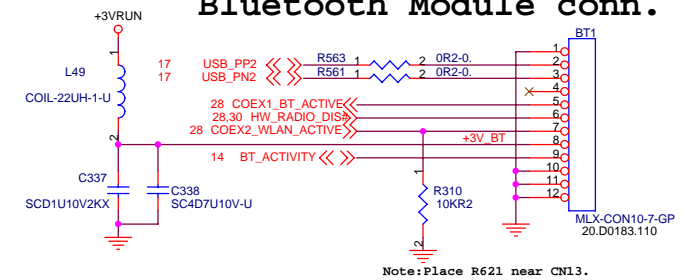
Dual USB1_VCC switch for USB4/USB5



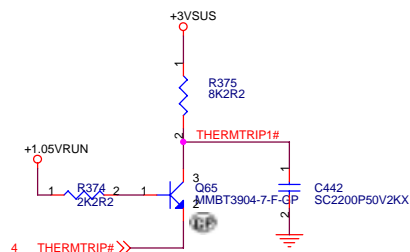
Modem Connector (Not Standard Type)



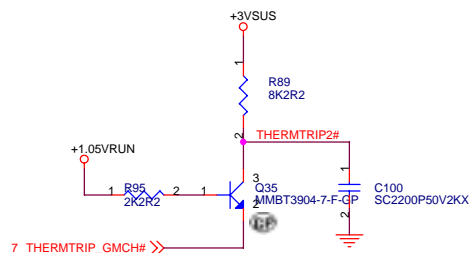
Bluetooth Module conn.



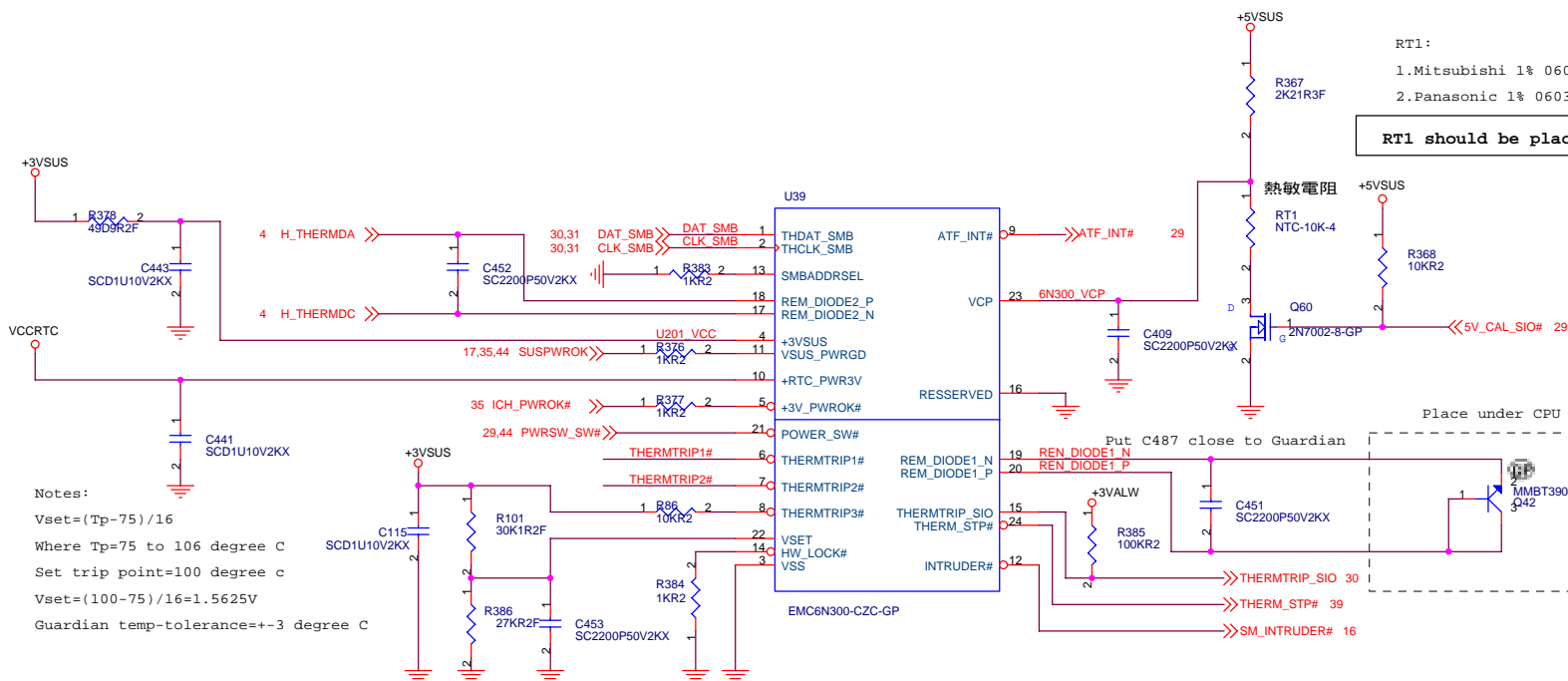
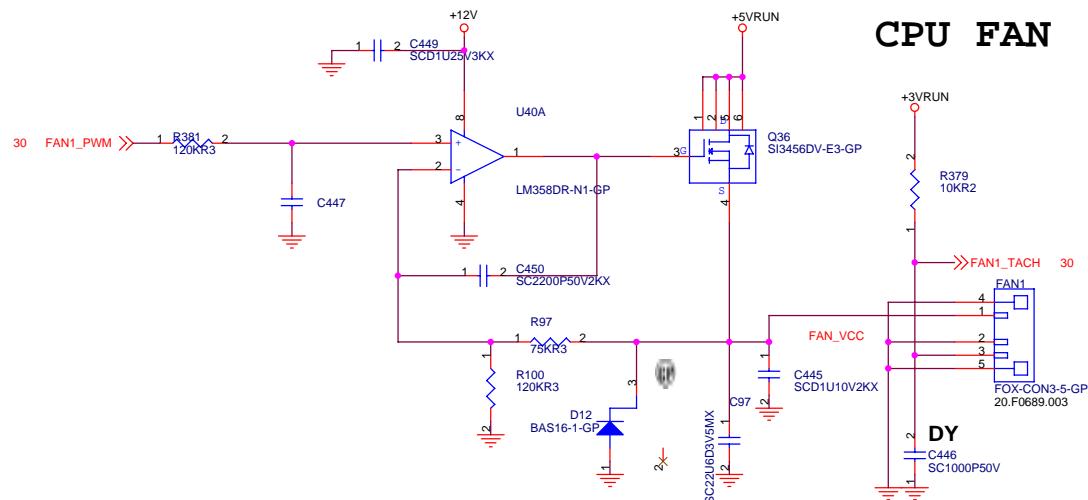
CPU FAN



C476 needs to be placed near Guardian IC.



7 THERMTRIP_GMCH#



Notes:
 $V_{set} = (T_p - 75) / 16$
 Where $T_p = 75$ to 106 degree C
 Set trip point = 100 degree c
 $V_{set} = (100 - 75) / 16 = 1.5625V$
 Guardian temp-tolerance = ± 3 degree C

RT1:
 1. Mitsubishi 1% 0603 10K ohm@25 degree C. P/N:TH11-3h103FT
 2. Panasonic 1% 0603 10K ohm@25 degree C. P/N:ERTJ1VGI03FA

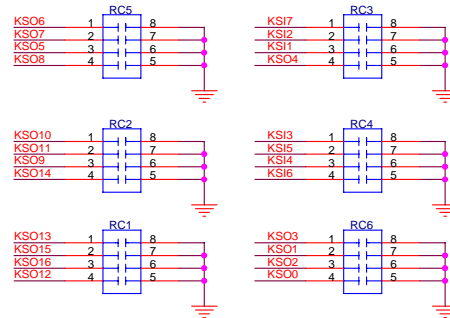
RT1 should be placed on bottom side of MB and sodimm

Place under CPU

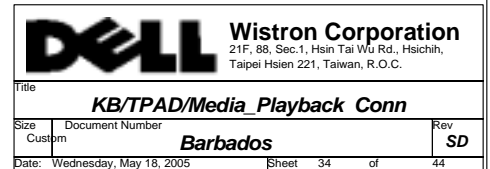
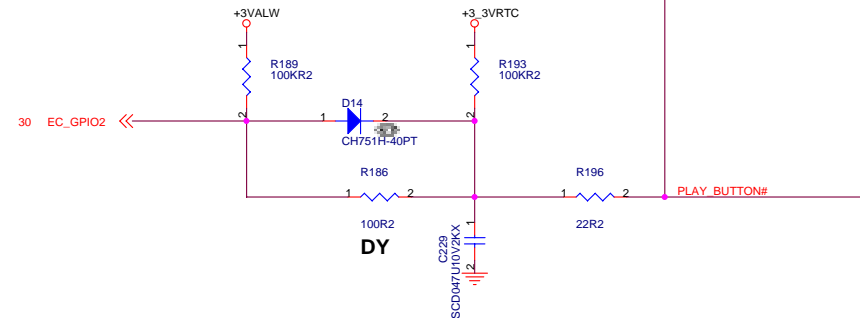
Put C487 close to Guardian

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MC6N300, Fan Control		
Size: A3	Document Number: Barbados	Rev: SD
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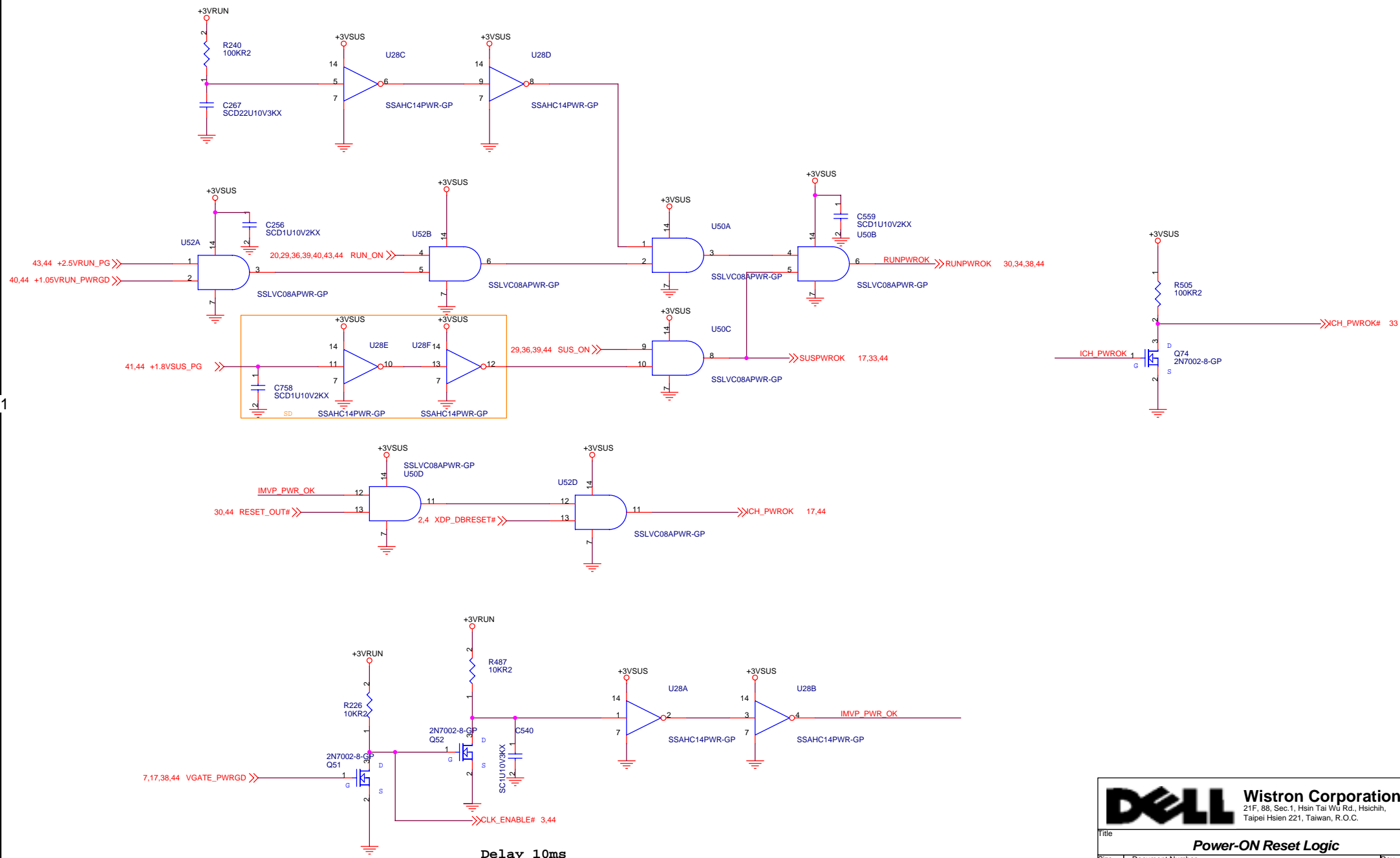
Media PlayBack / TouchPAD Connector

[illegible]

PLAY_PWR	PLAY_Button#
LOW	Regular Play Function
HIGH	Power On Function

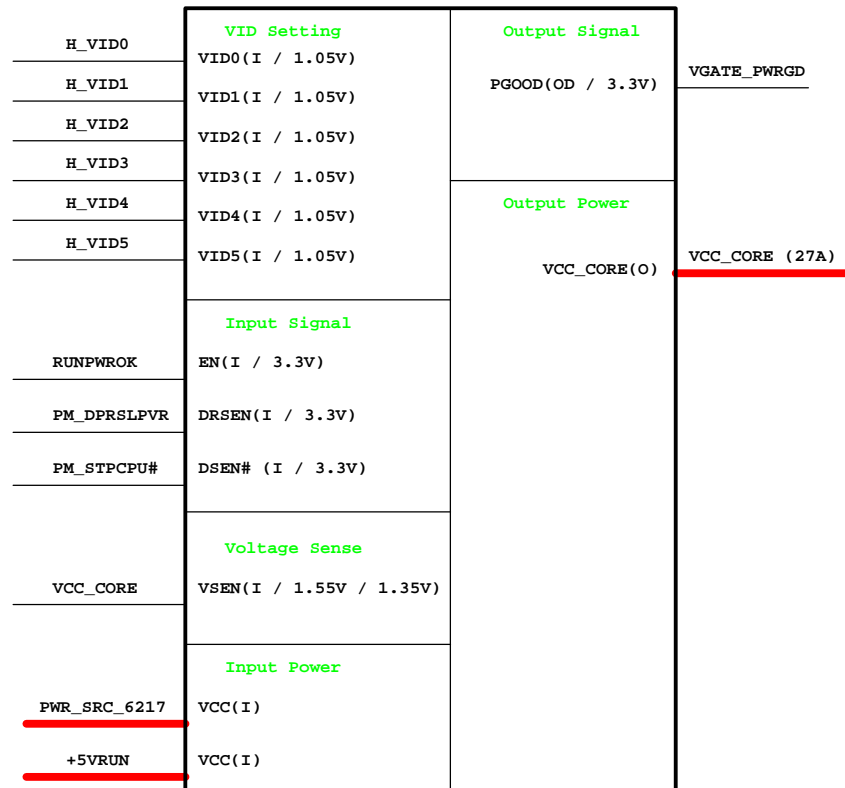


A

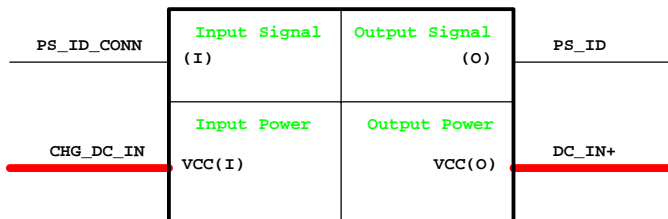


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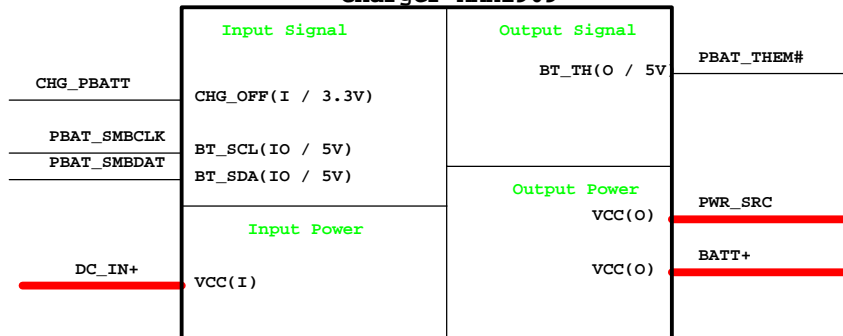
CPU_CORE ISL6217A



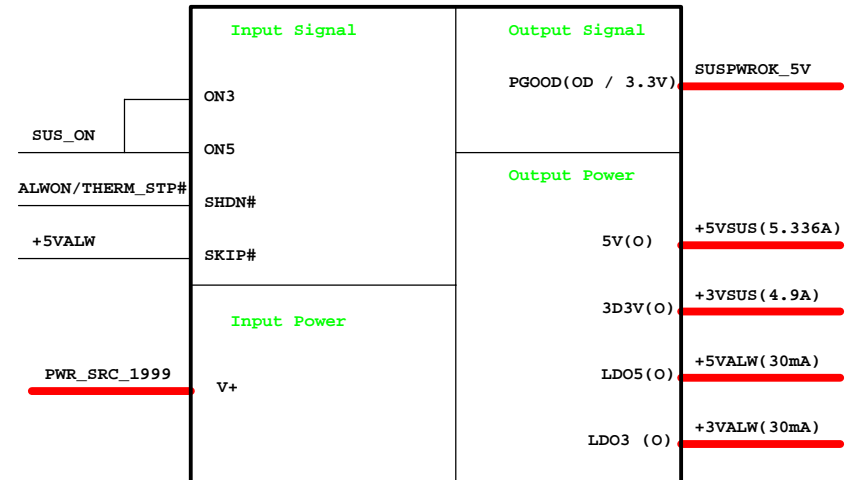
Adapter



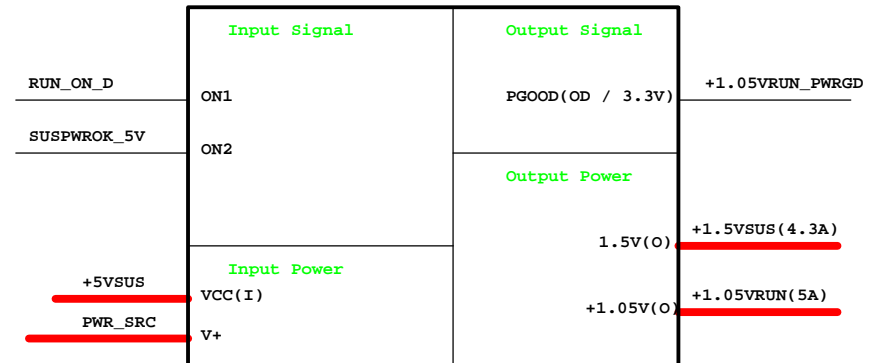
Charger MAX1909



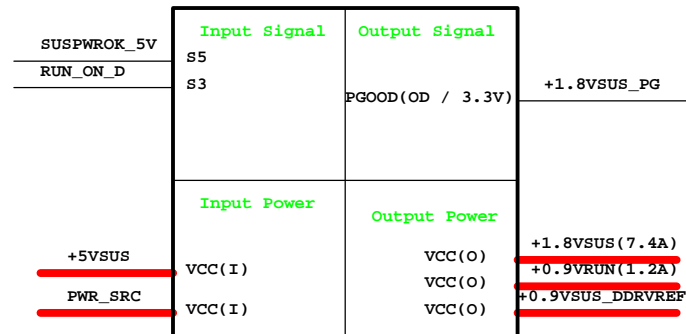
Max8734A 5V/3D3V

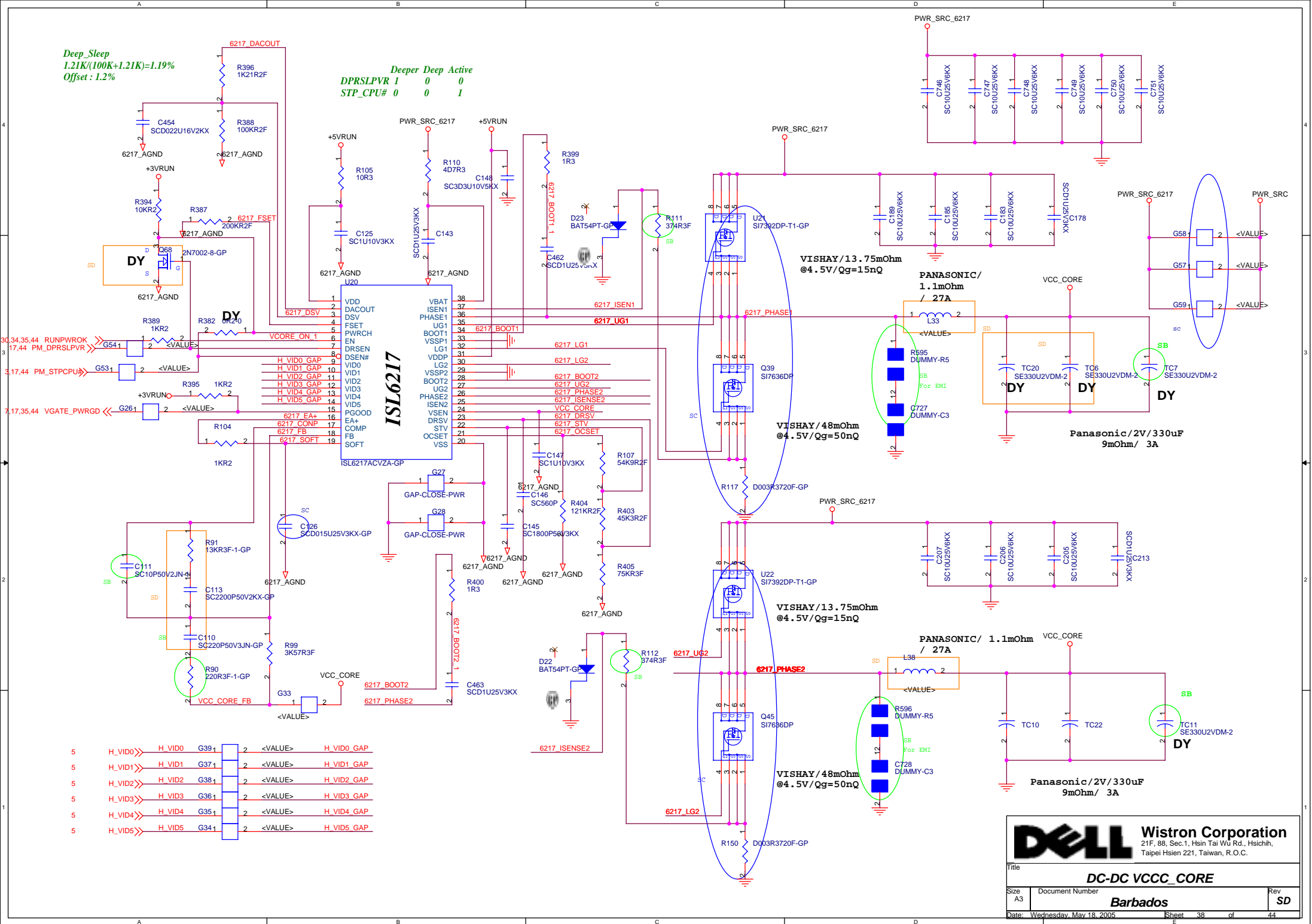


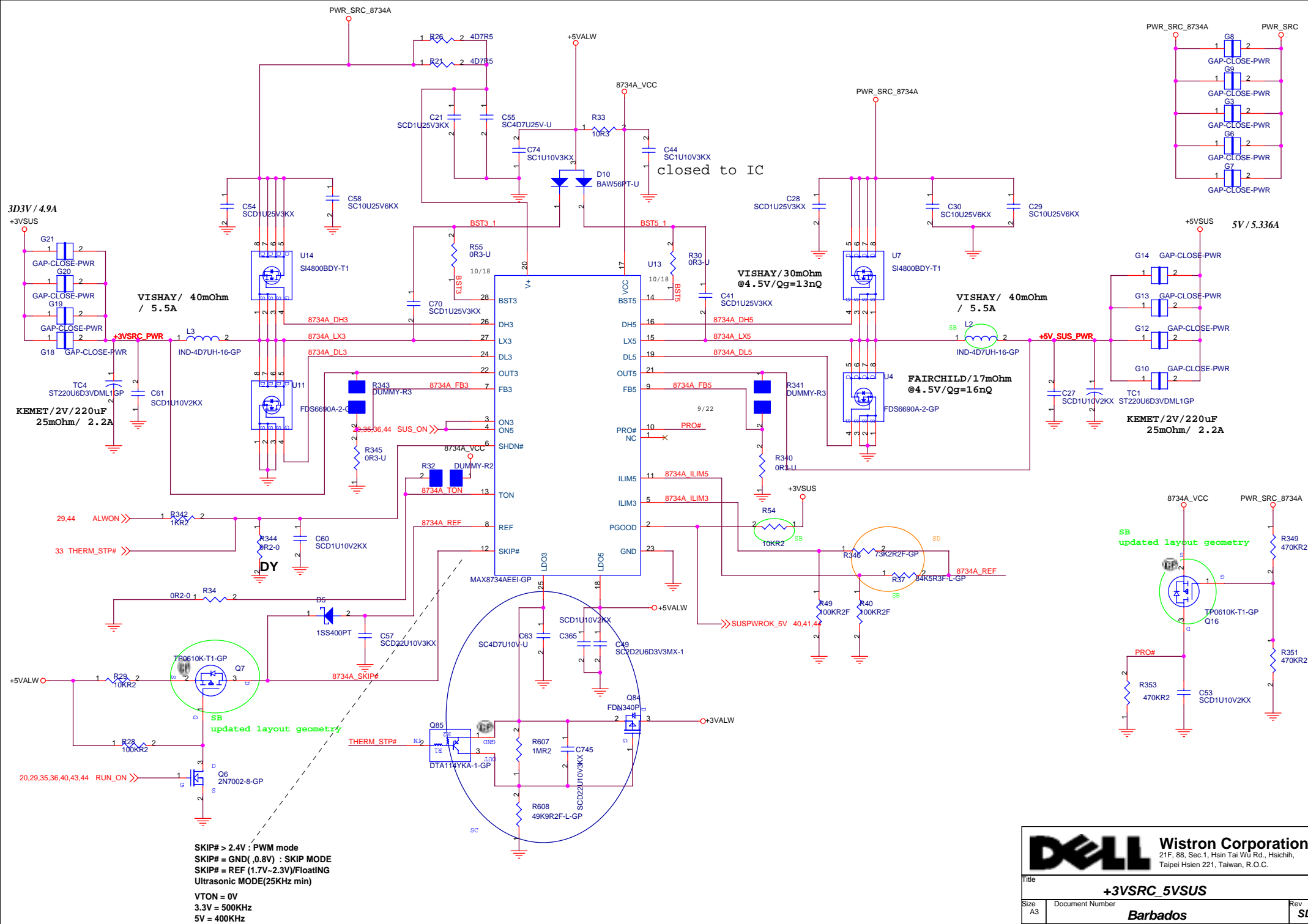
Max8743 1.5V/1.05V



TI51116 1.8V / 0.9V

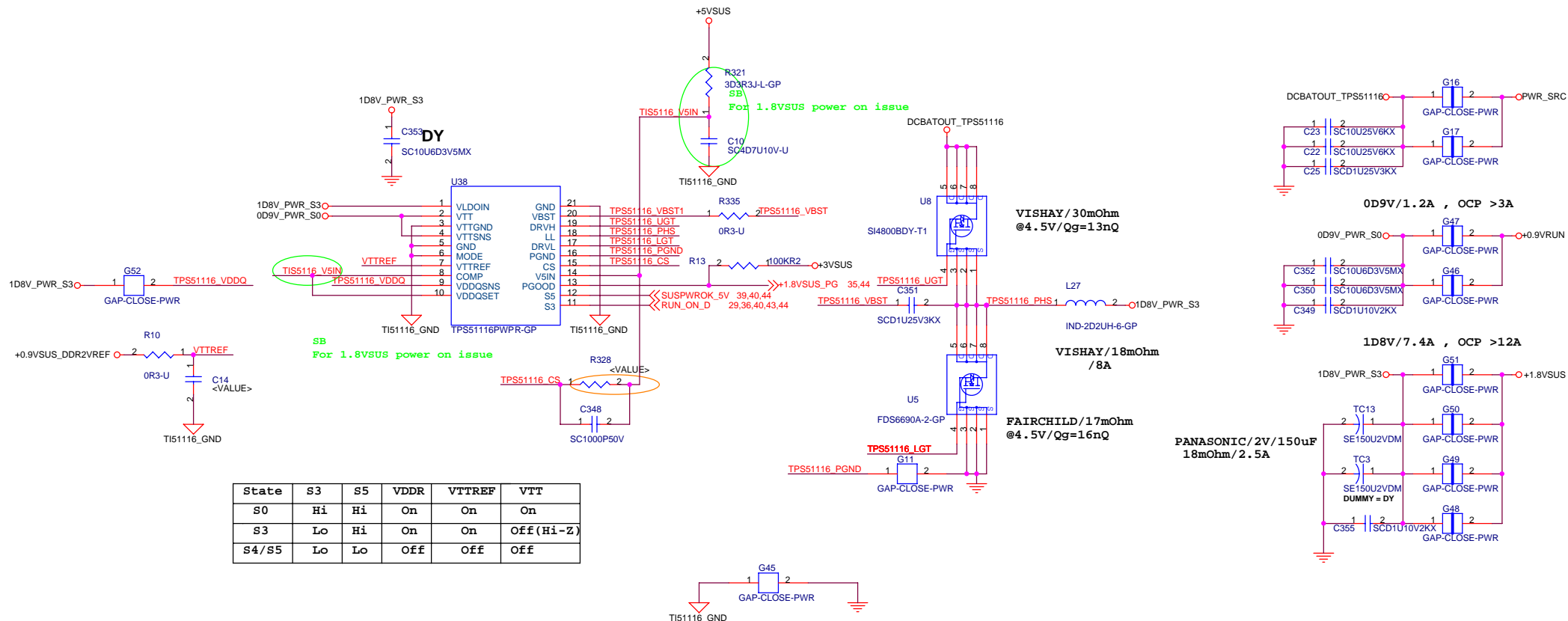








TI TPS51116 for 1D8V and 0D9V

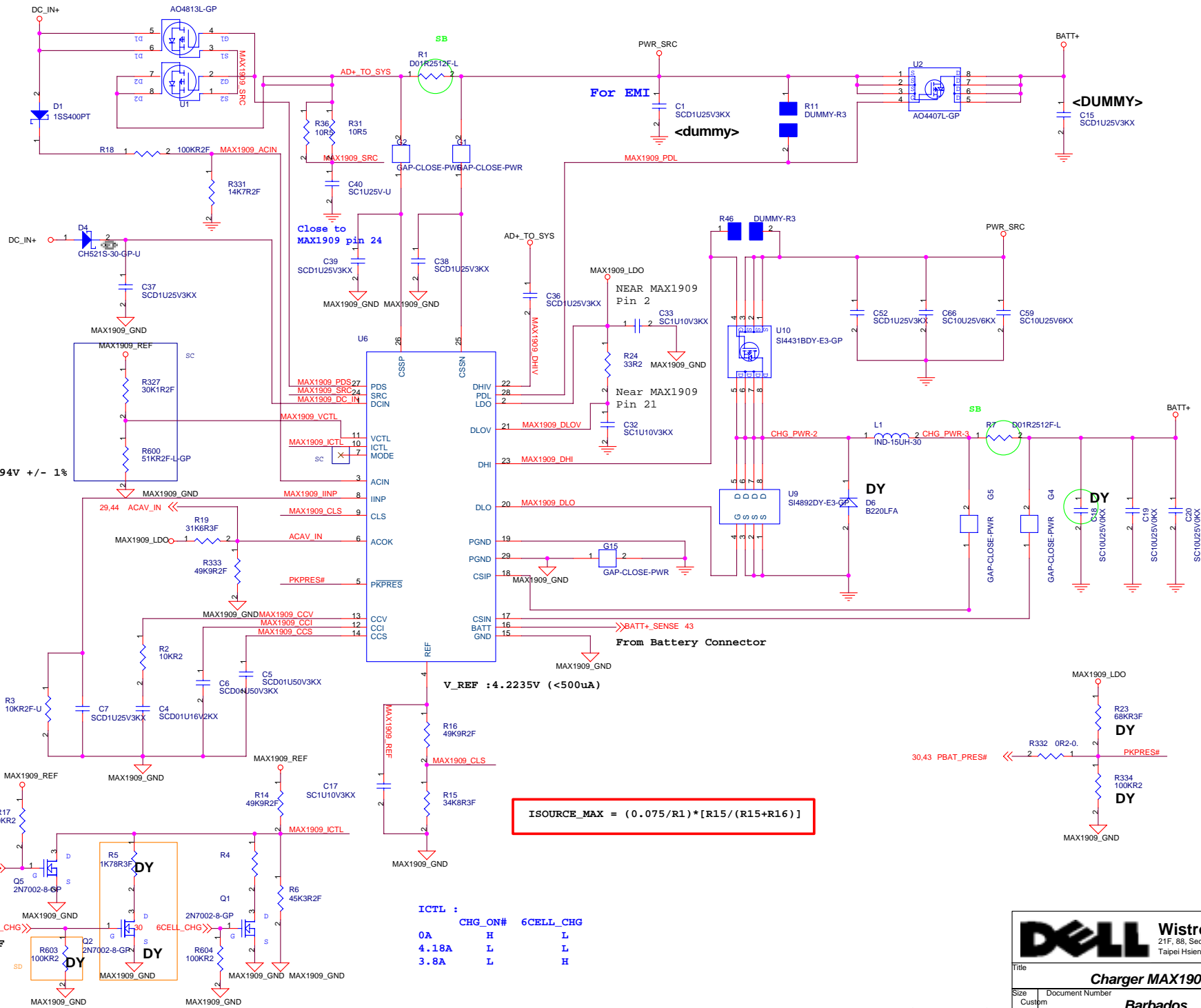


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT

MAX1909_VCTL
Typ. Voltage = 12.94V +/- 1%

CHG_PBATT# is H:
Charge OFF
CHG_PBATT# is L:
Charge ON



$$ISOURCE_MAX = (0.075/R1) * [R15/(R15+R16)]$$

ICTL :

CHG_ON#	6CELL_CHG
0A	H
4.18A	L
3.8A	L



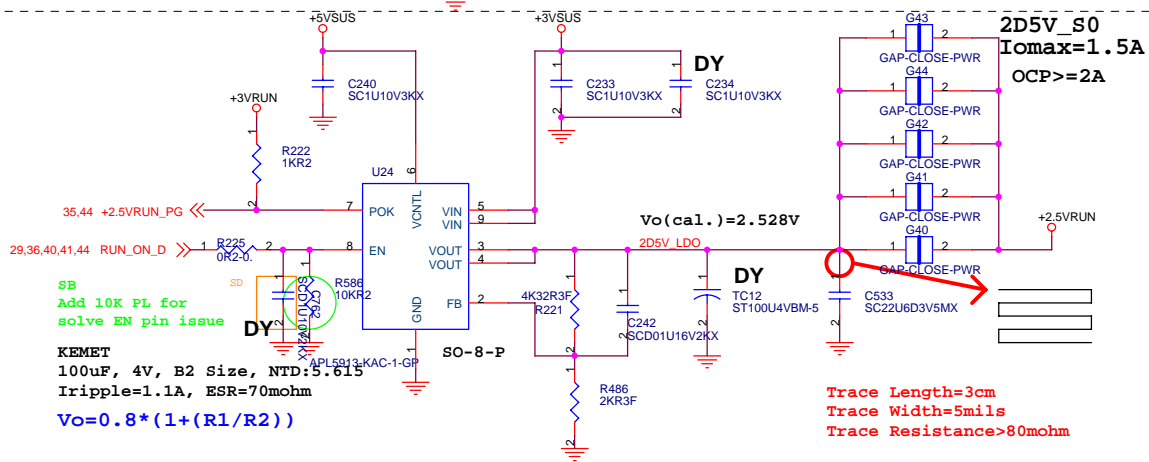
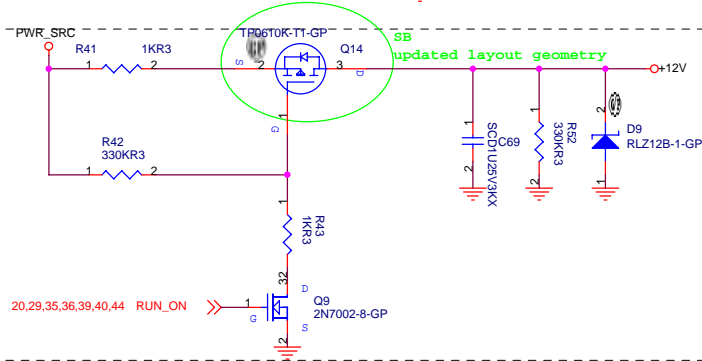
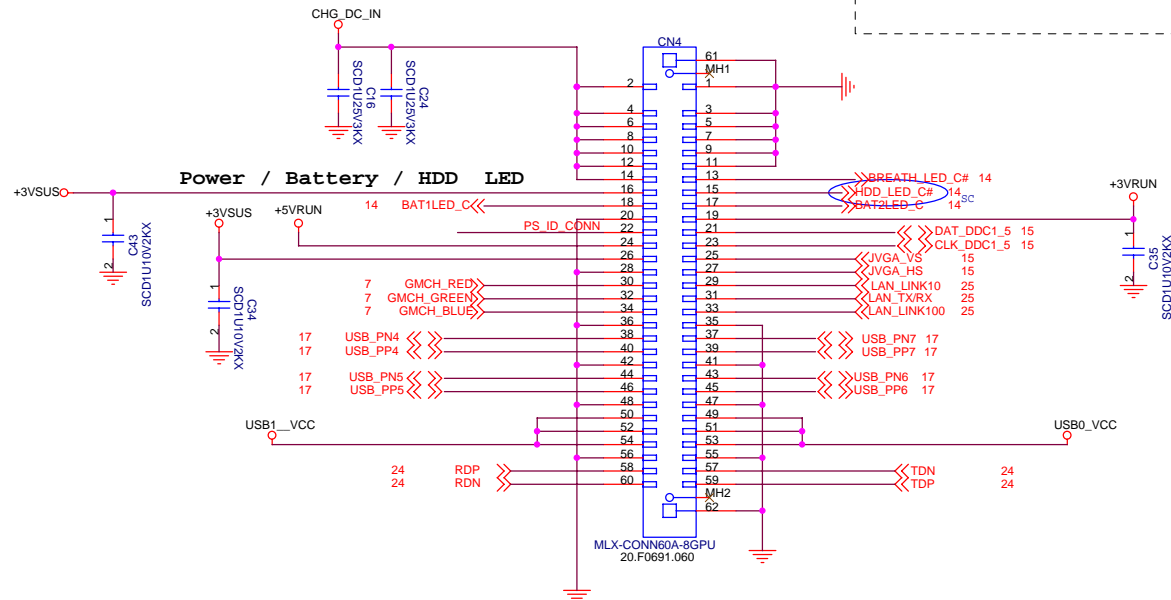
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Charger MAX1909	
Size	Document Number	Barbados		Rev
Custom				SD
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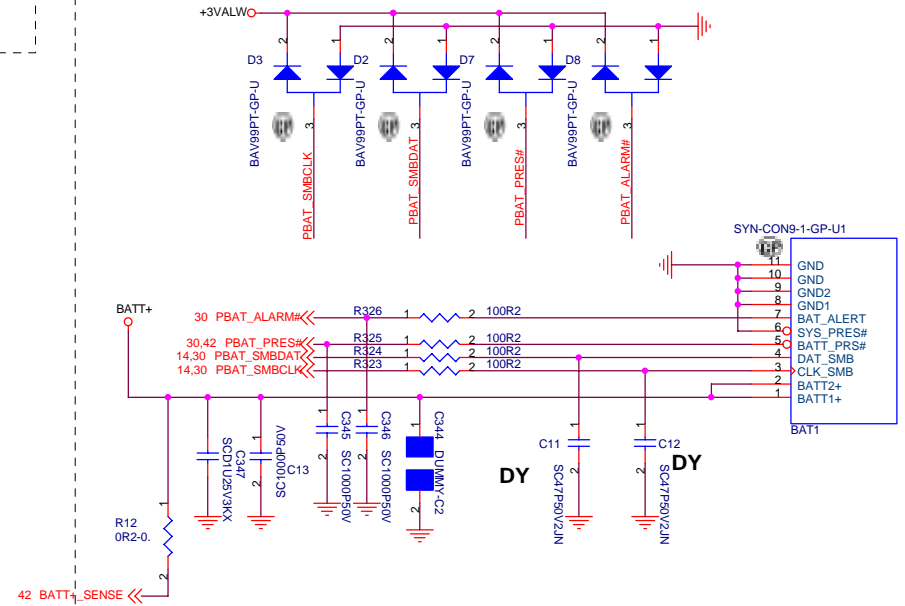
(Power Team)

TV BD Conn

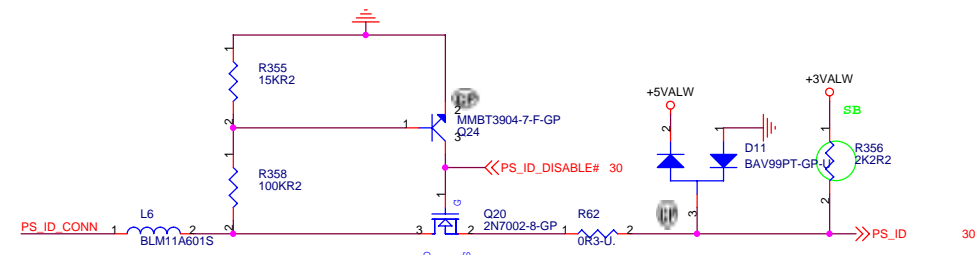
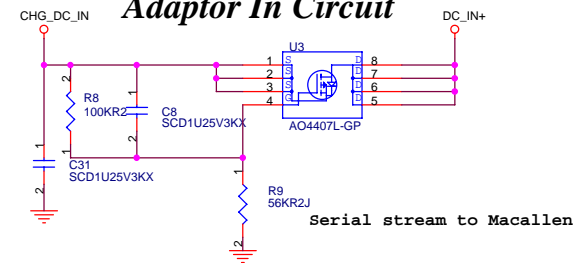
Layout Note:
Must be a ground return path for
CRT_R,CRT_G,CRT_B



Battery Conn



Adaptor In Circuit



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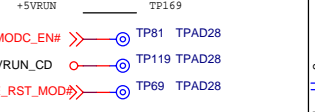
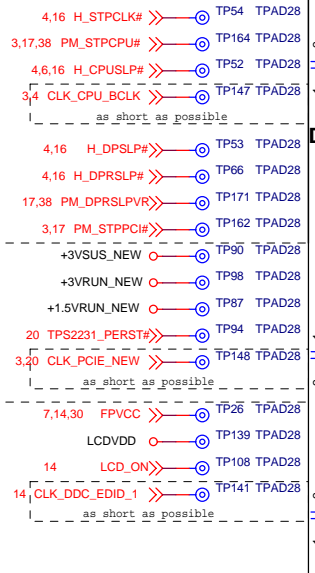
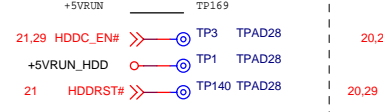
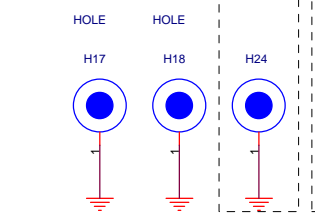
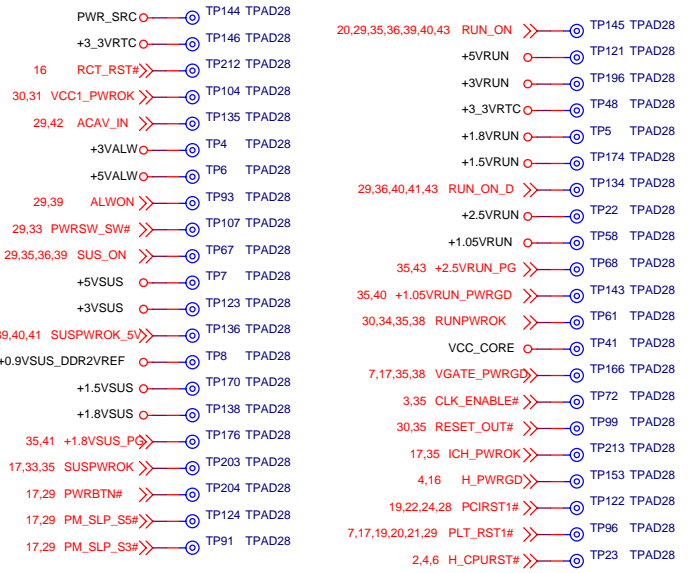
Title **Battery/TV/Adaptor Conn/+2.5VSUS**

Size A3	Document Number Barbados
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SD

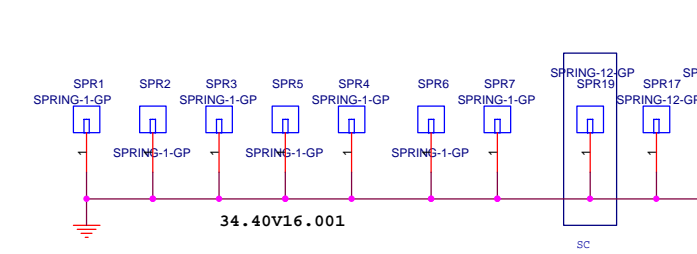
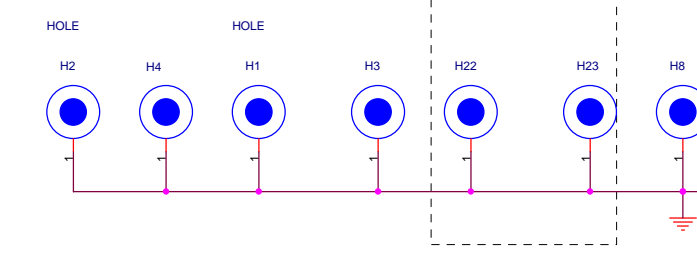
Date: Wednesday, May 18, 2005

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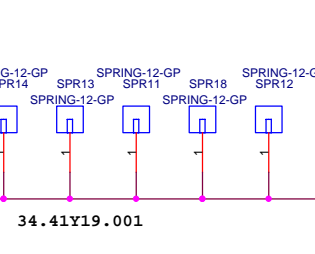
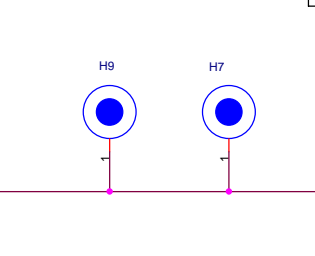
34.4C408.001
BOT SIDE

34.4C408.001
BOT SIDE

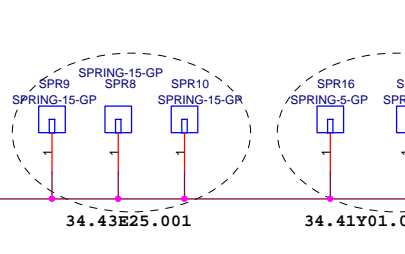
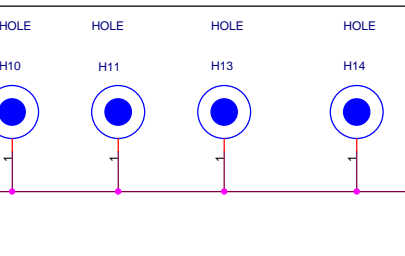
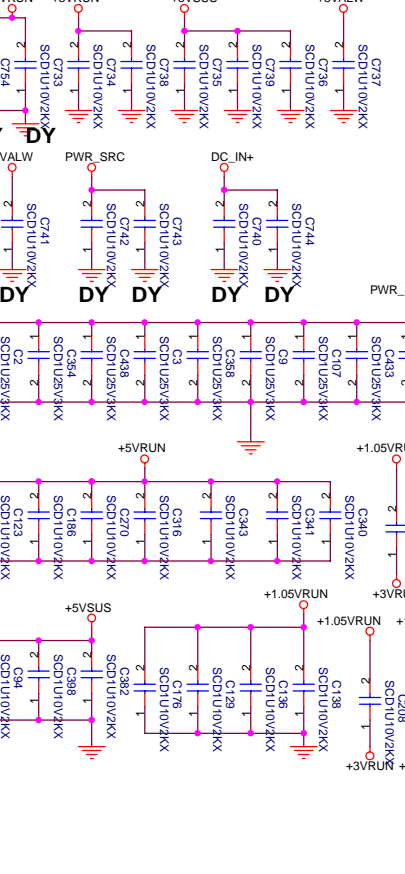


34.40V16.001

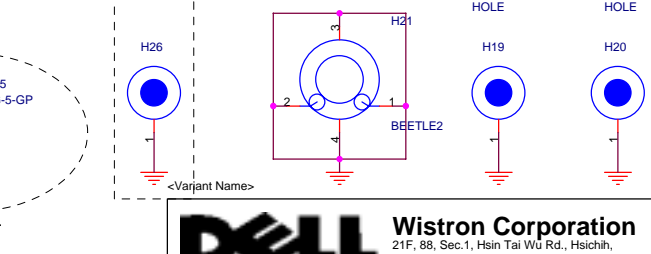
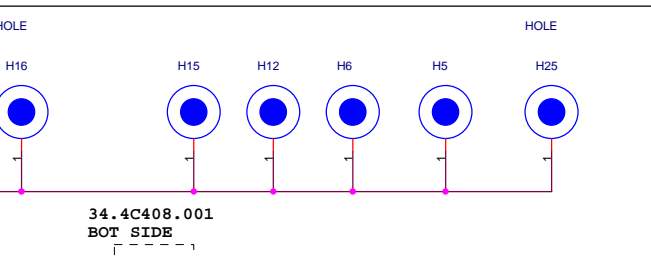
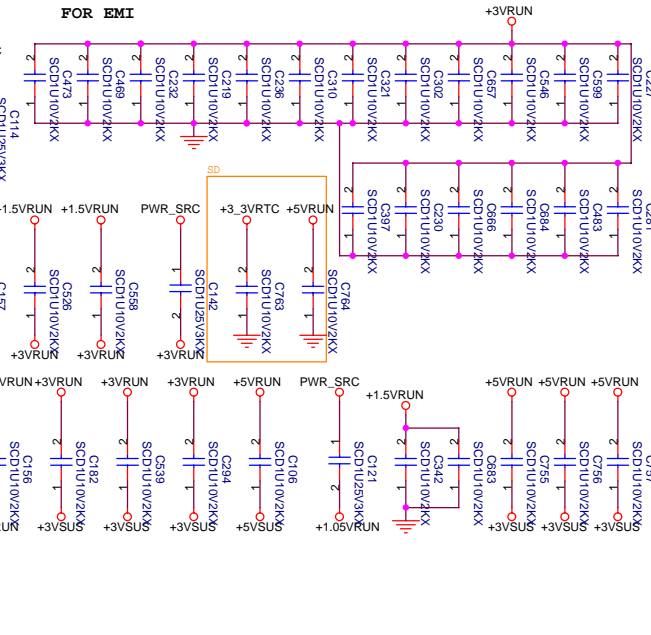
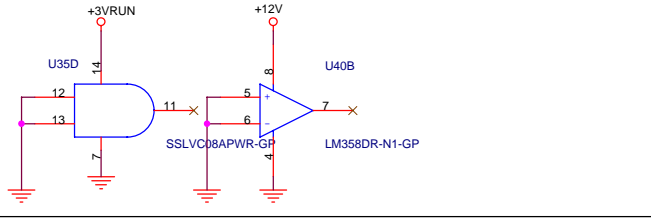
34.41Y19.001



34.43E25.001



34.41Y01.001



34.4C408.001
BOT SIDE